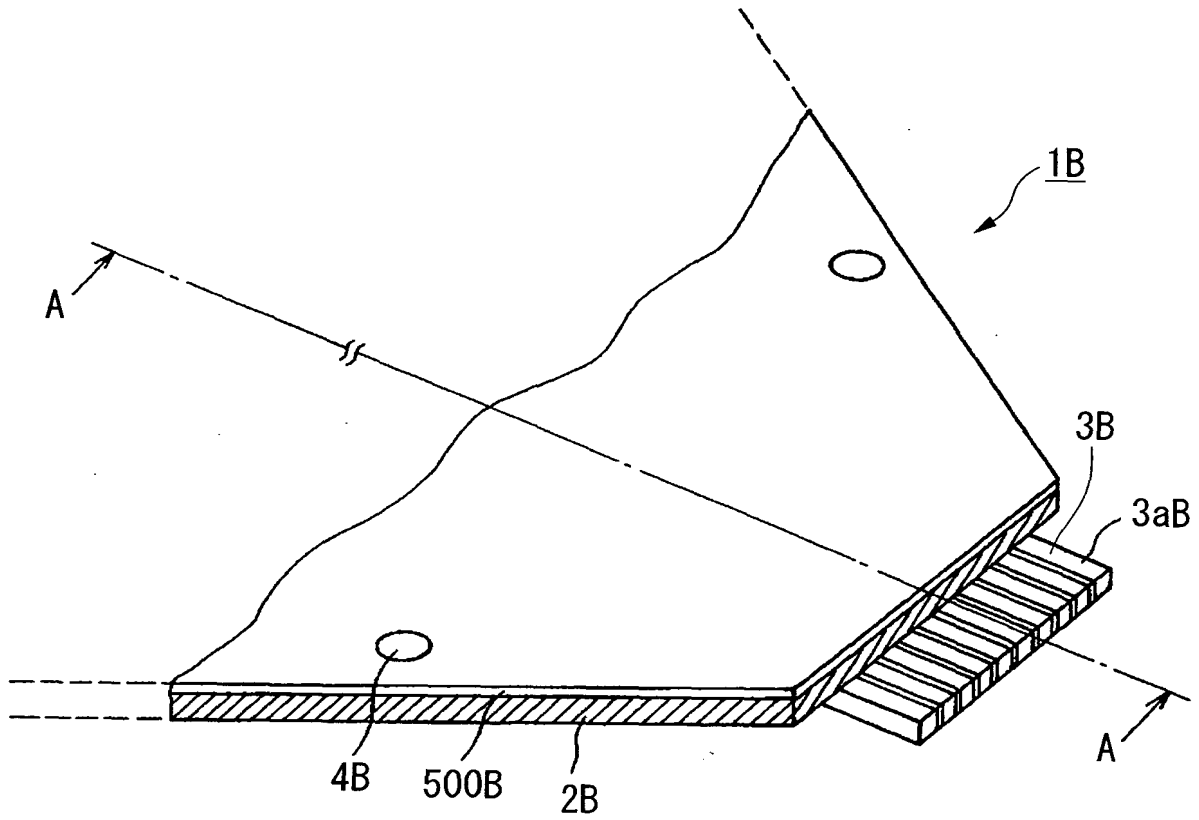
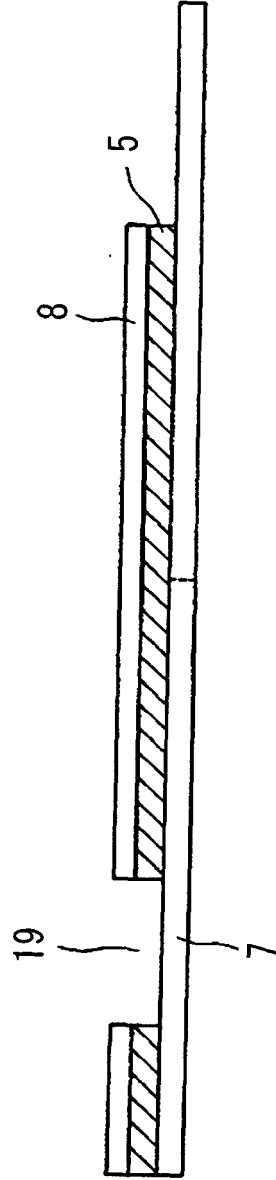


FIG. 1



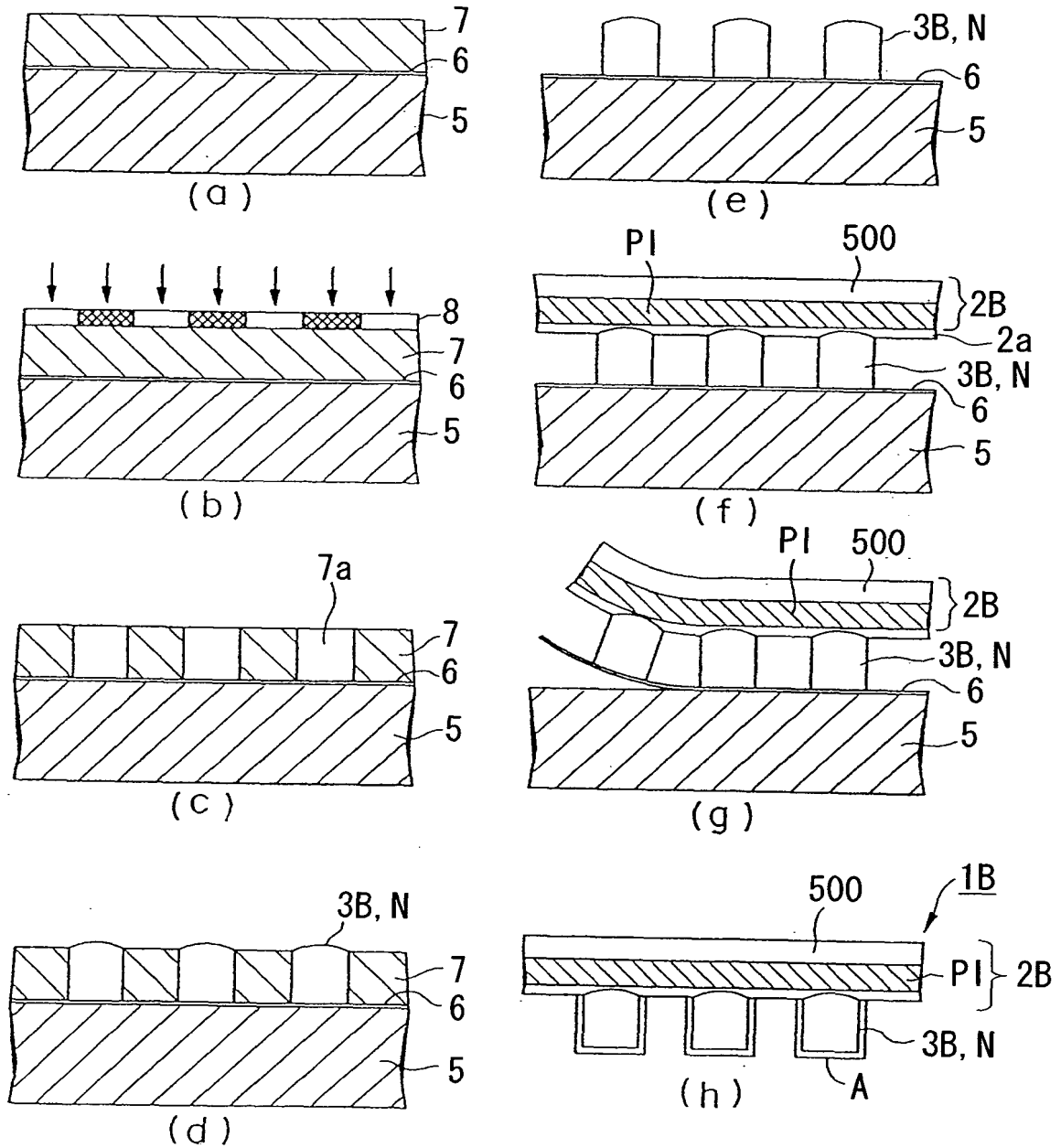
10076508-061902

FIG. 2



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FIG. 3



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FIG. 4

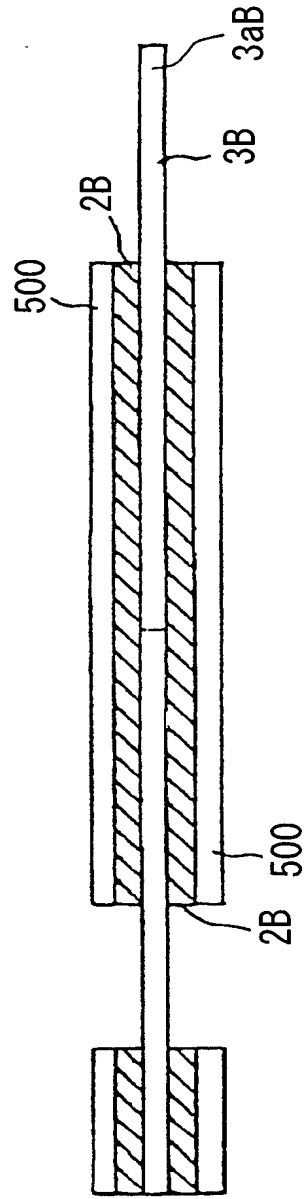


FIG. 5

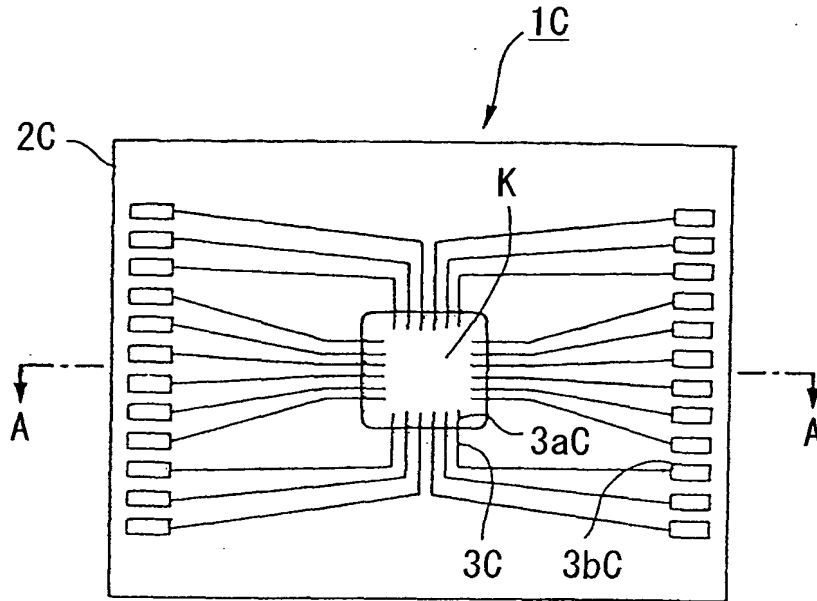


FIG. 6

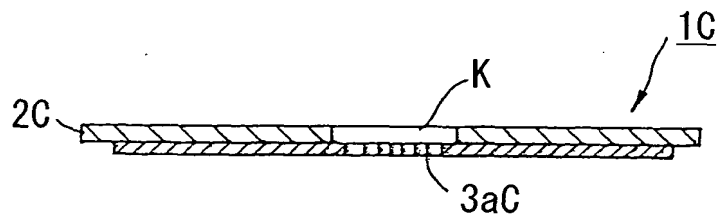
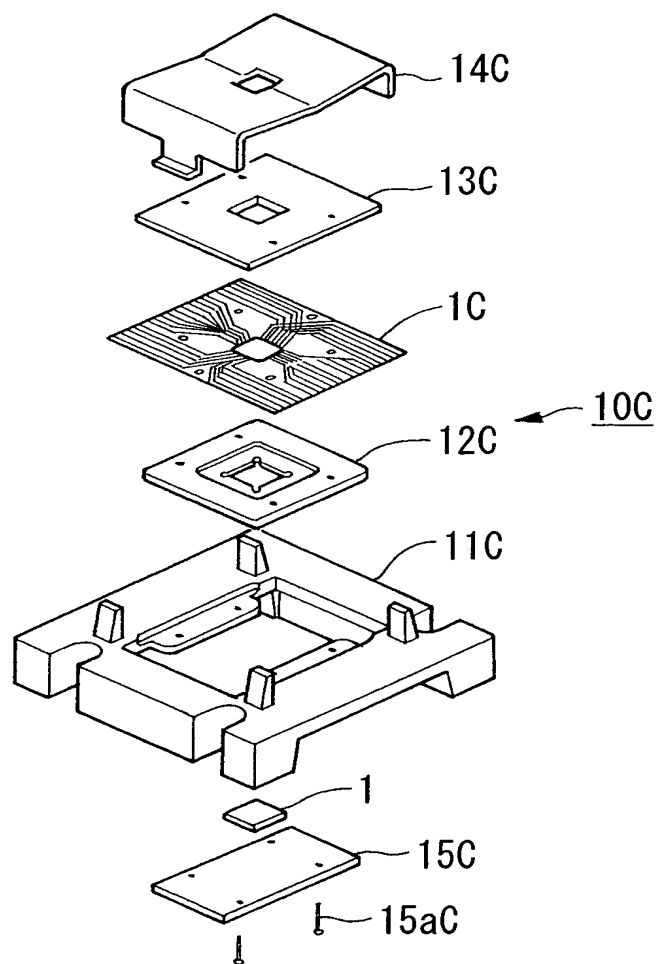


FIG. 7



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FIG. 8

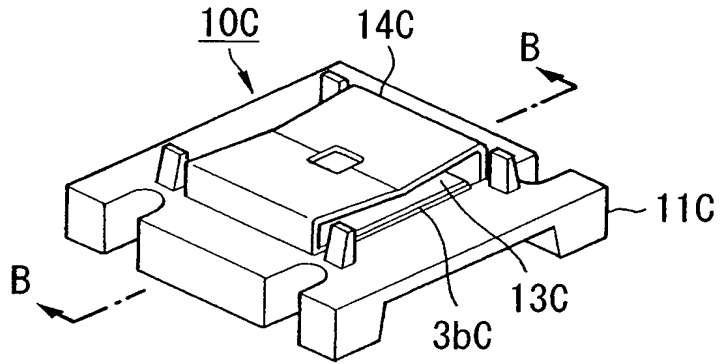


FIG. 9

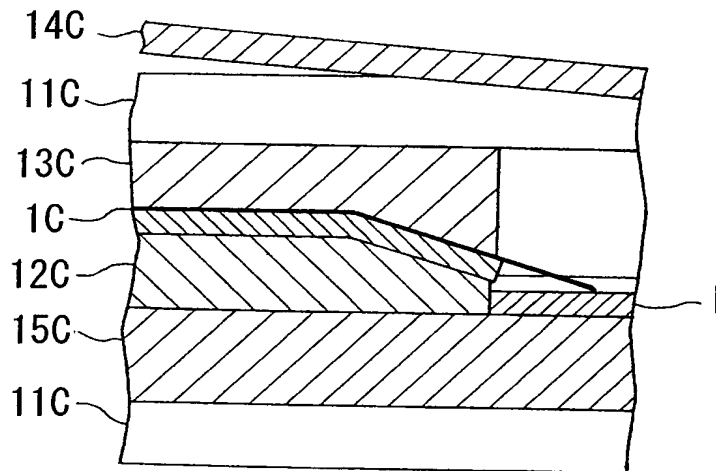


FIG. 10

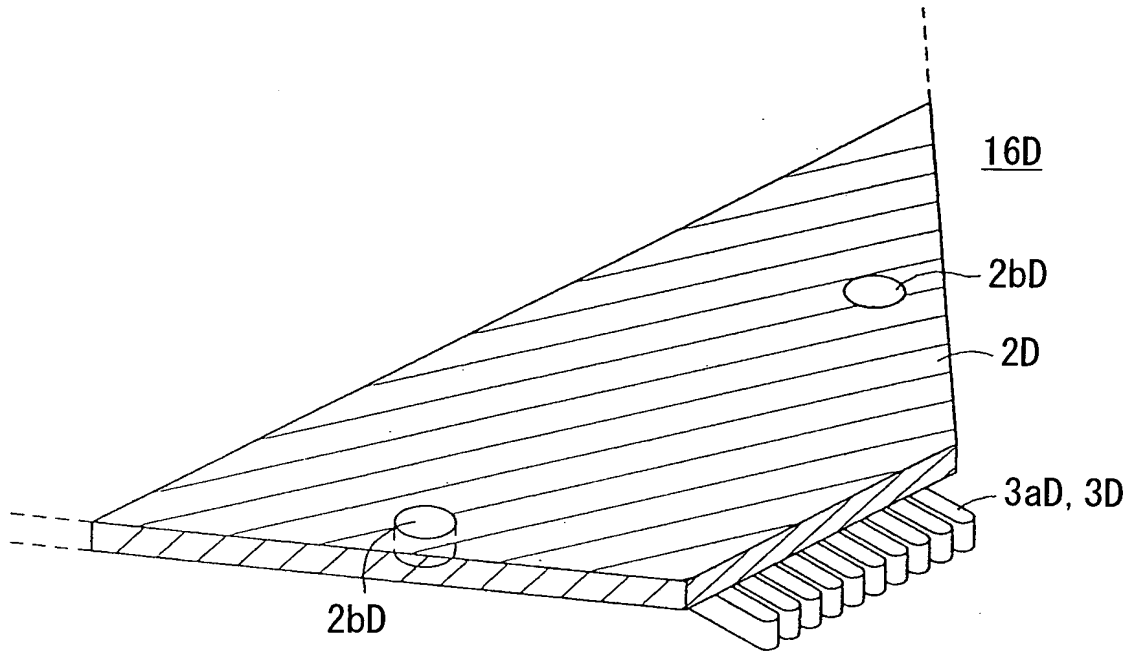


FIG. 11

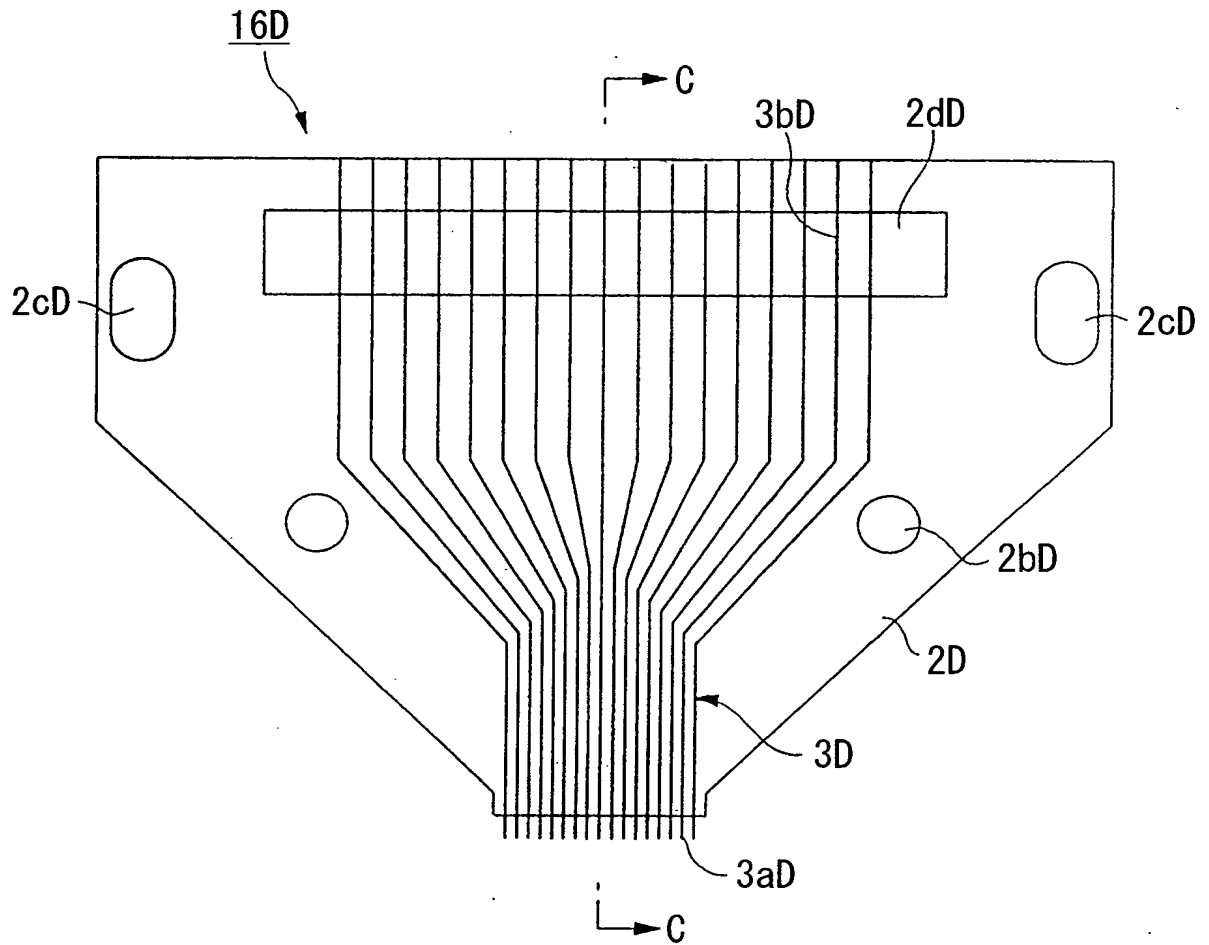


FIG. 12

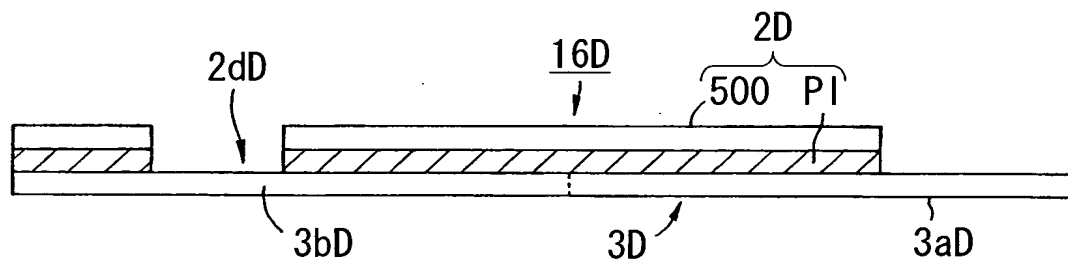
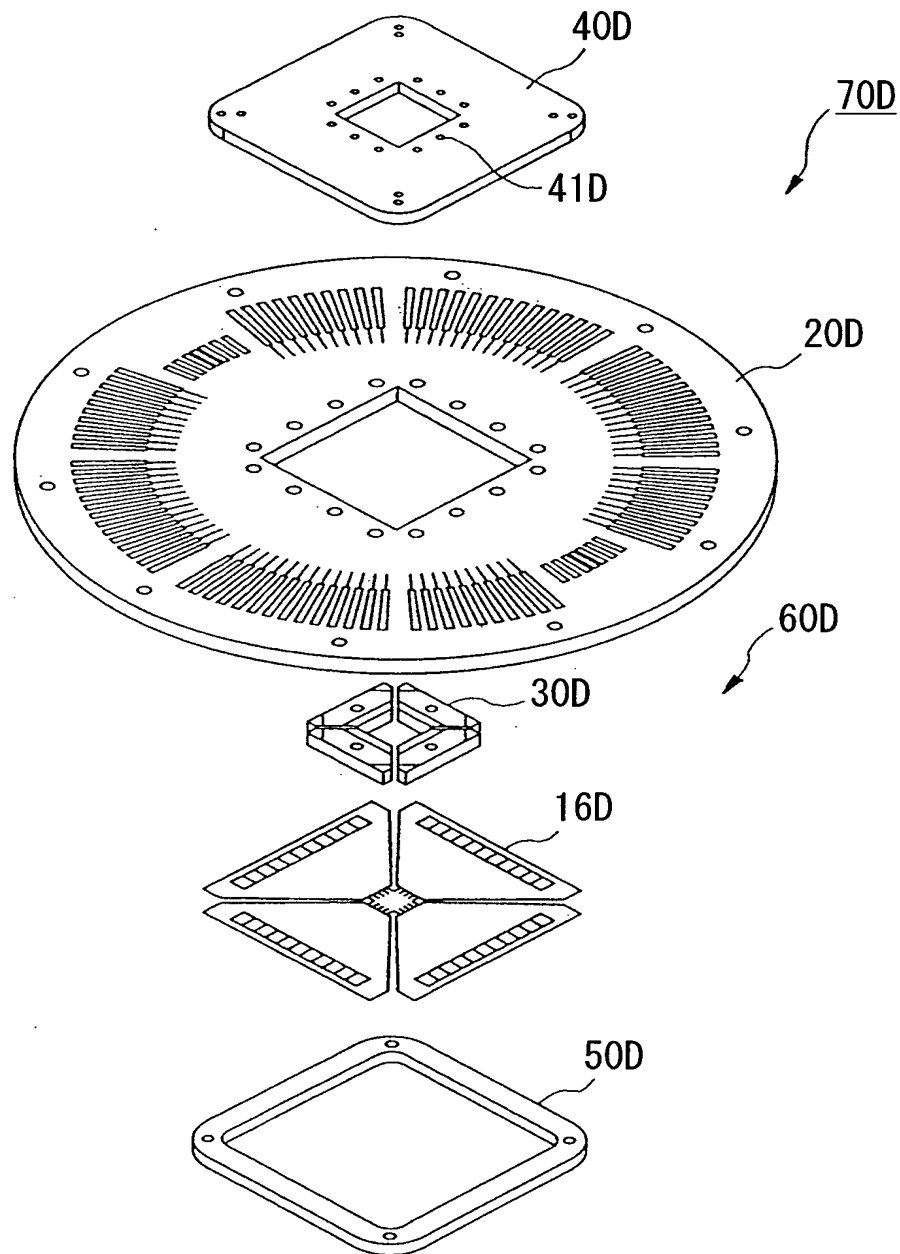


FIG. 13



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FIG. 14

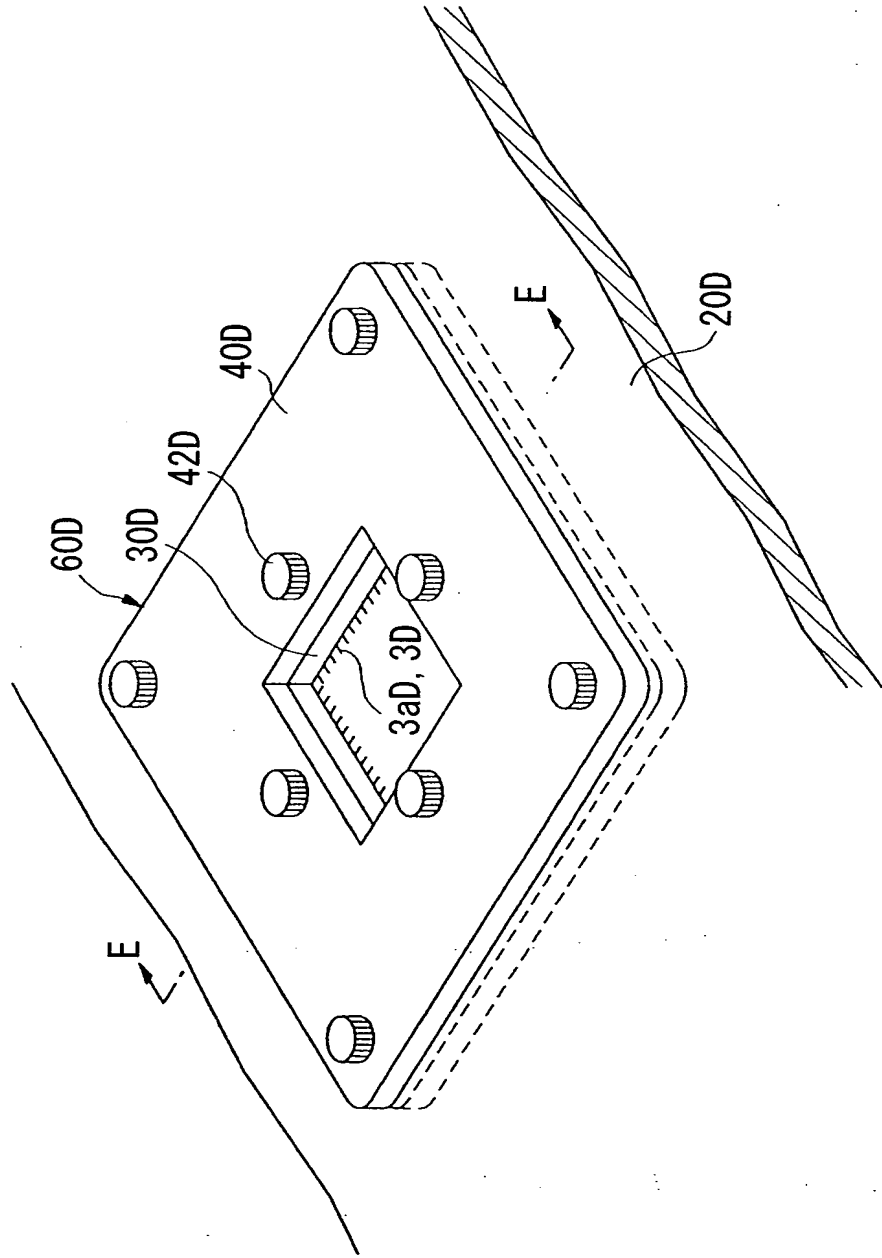


FIG. 15

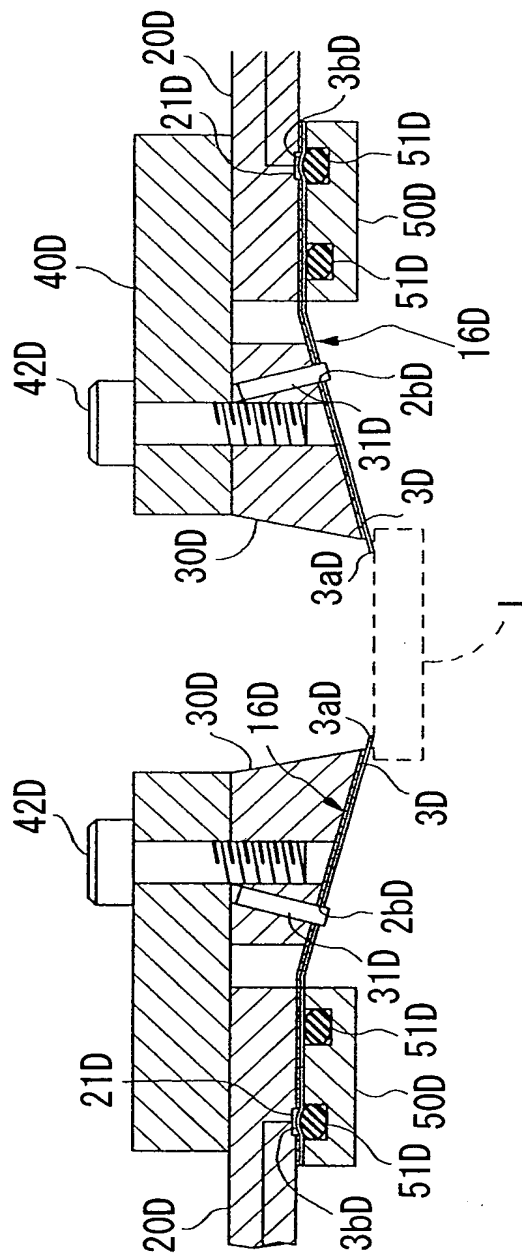


FIG. 16

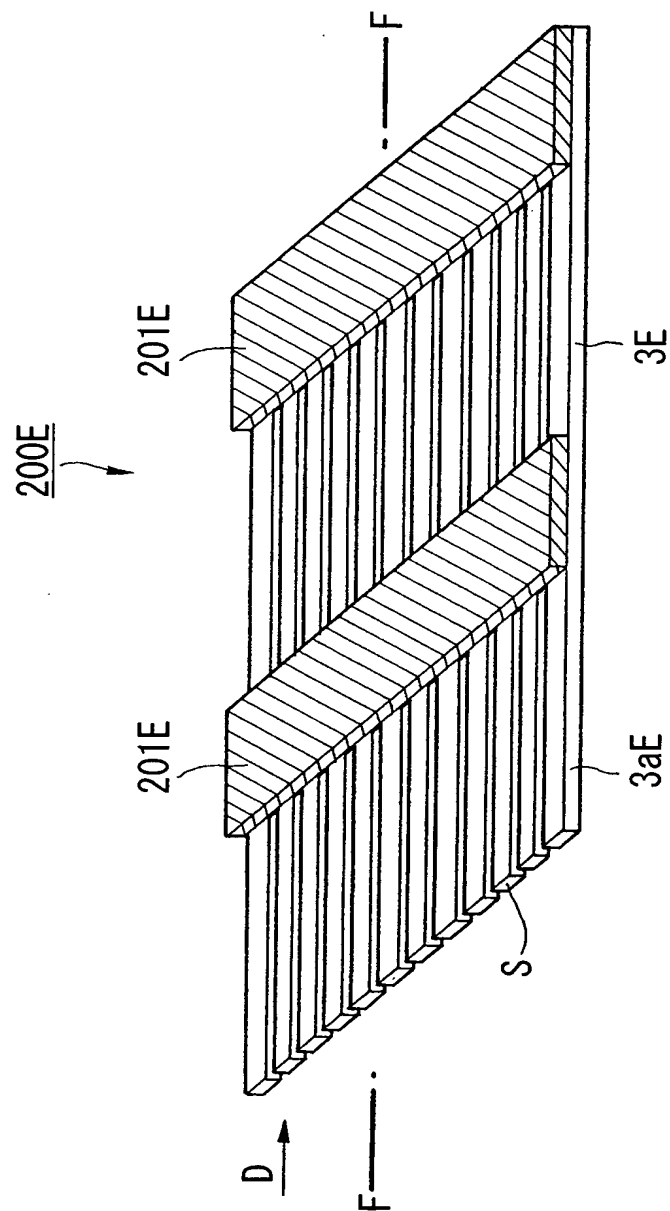
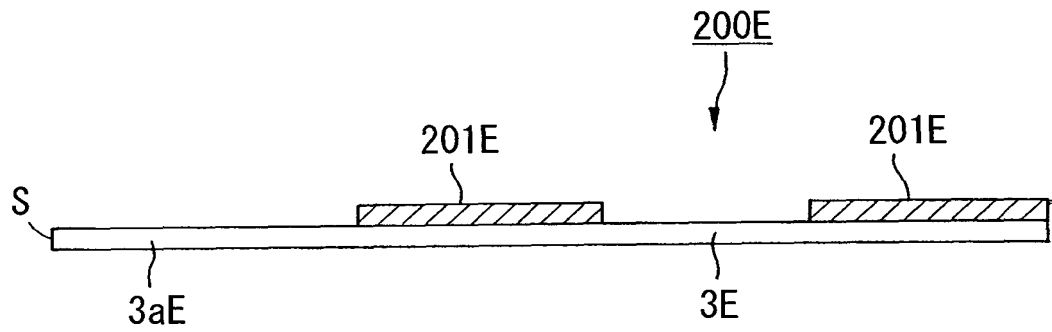
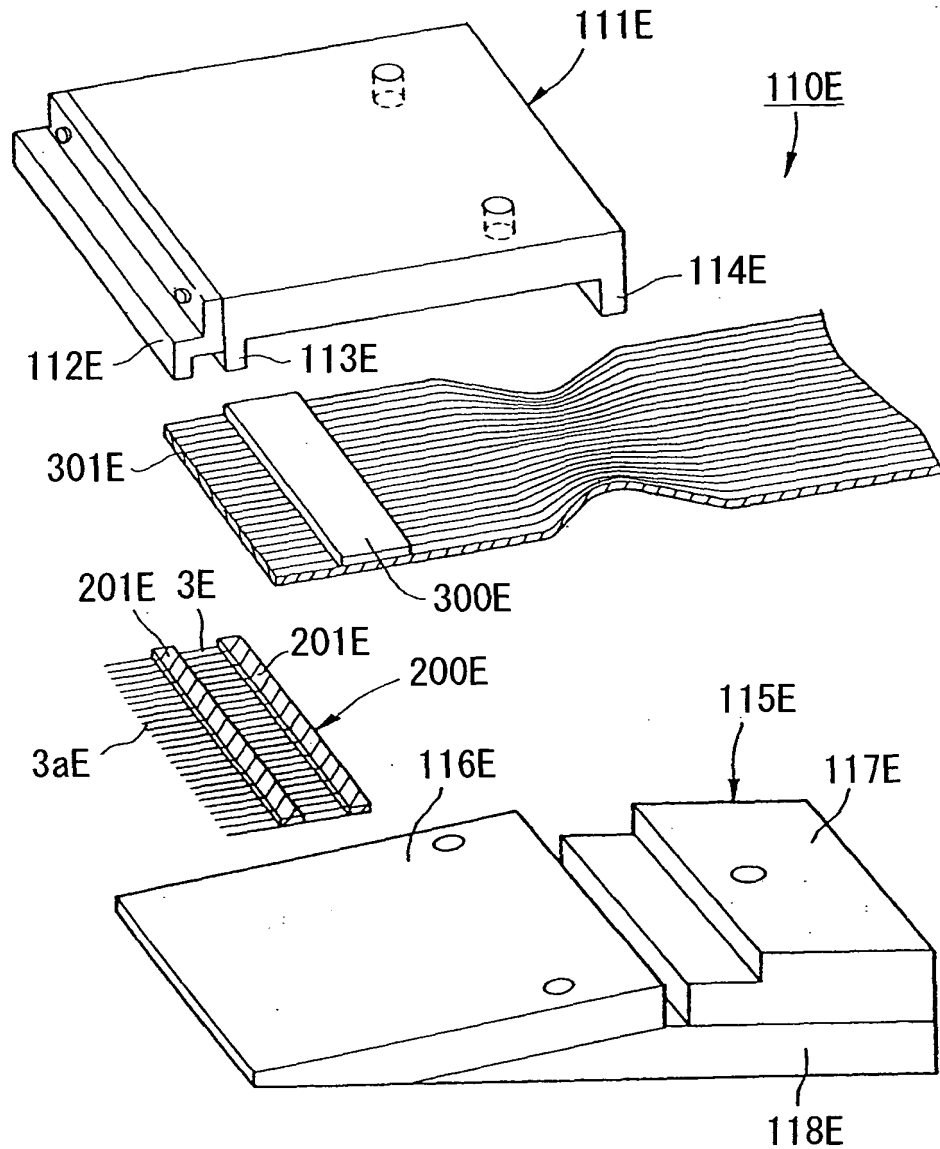


FIG. 17



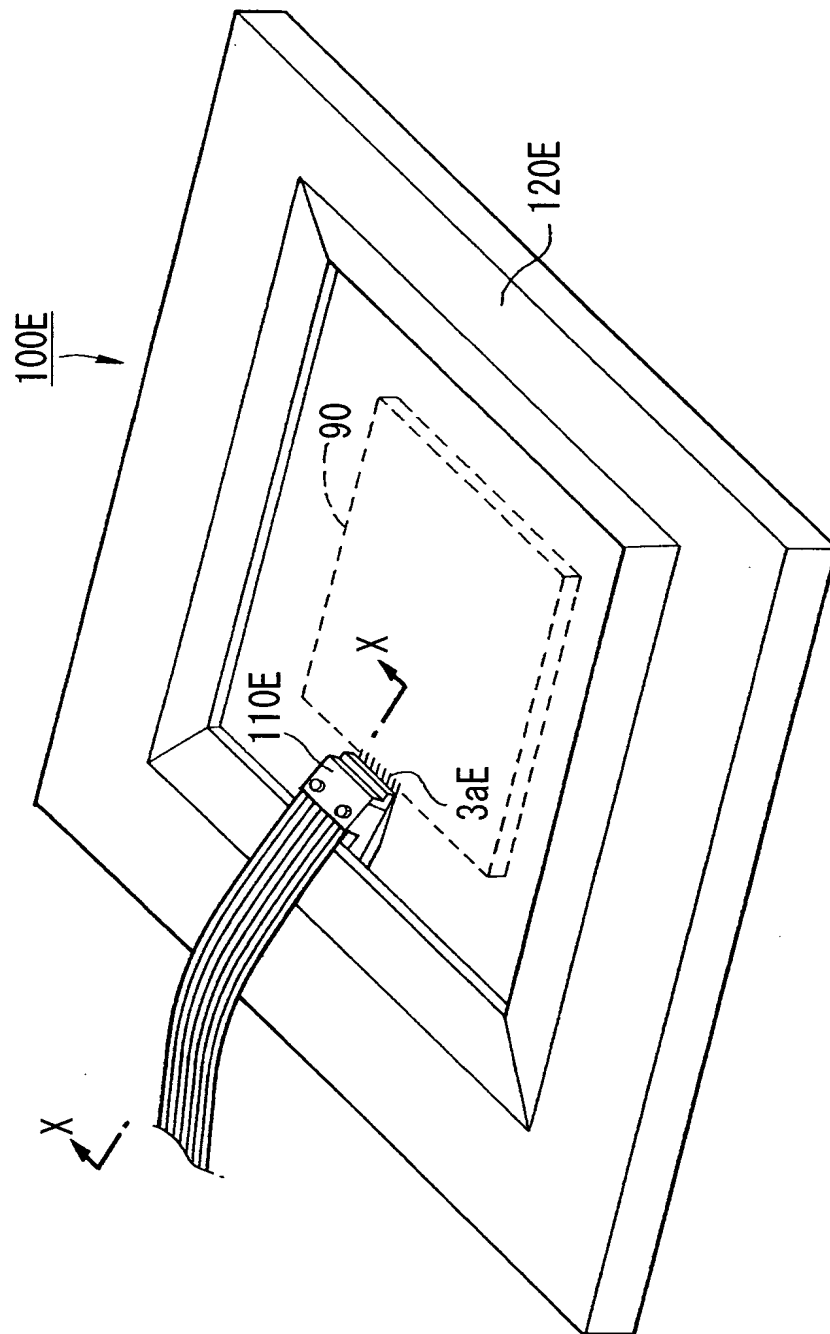
10076508-051902

FIG. 18



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FIG. 19



100E →

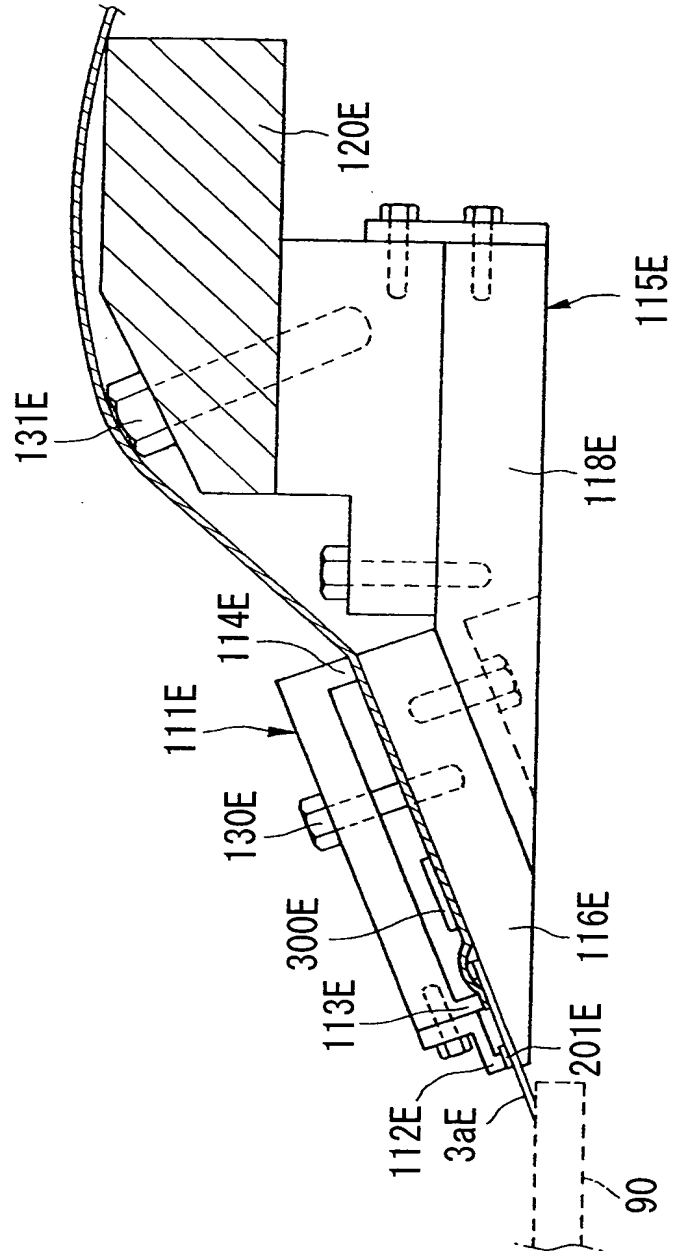


FIG. 22

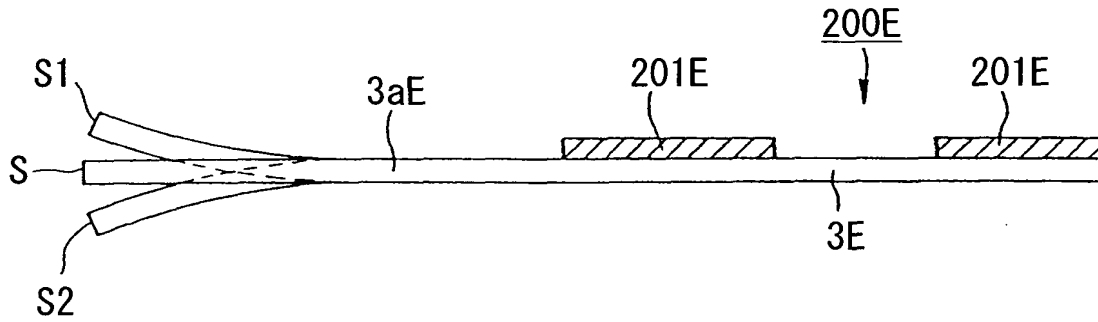
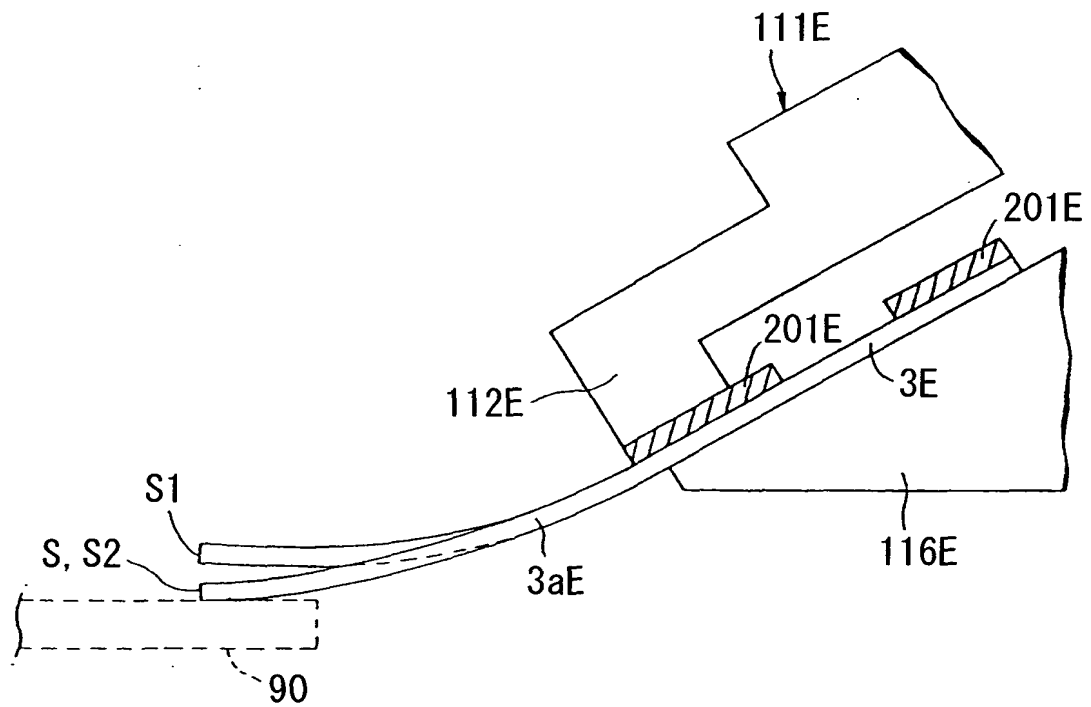


FIG. 23



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FIG. 24

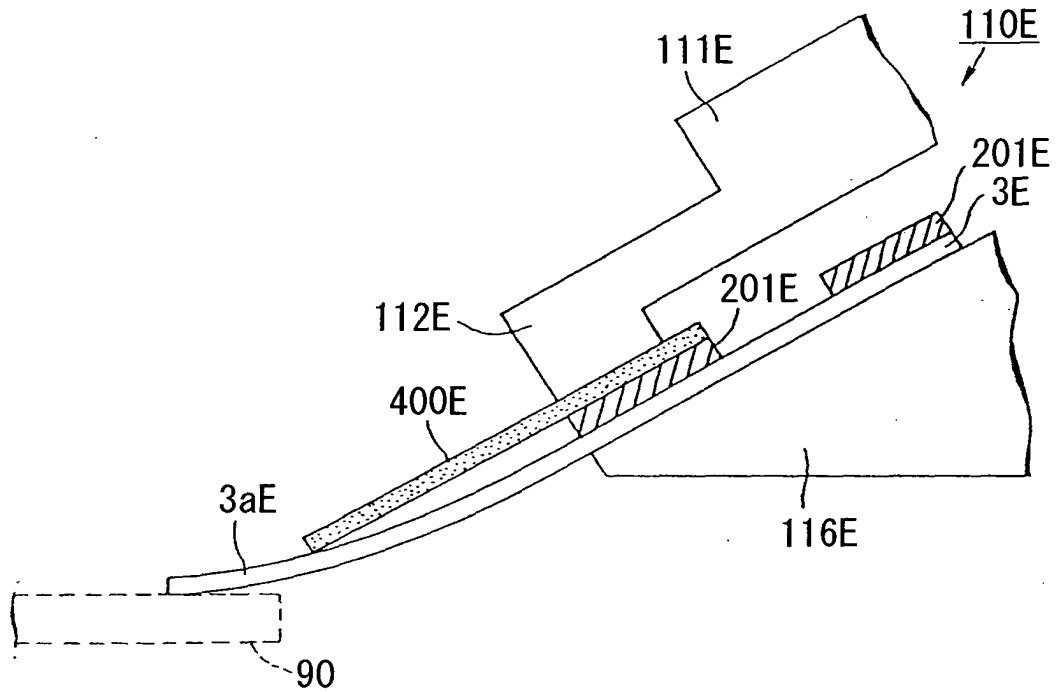


FIG. 25

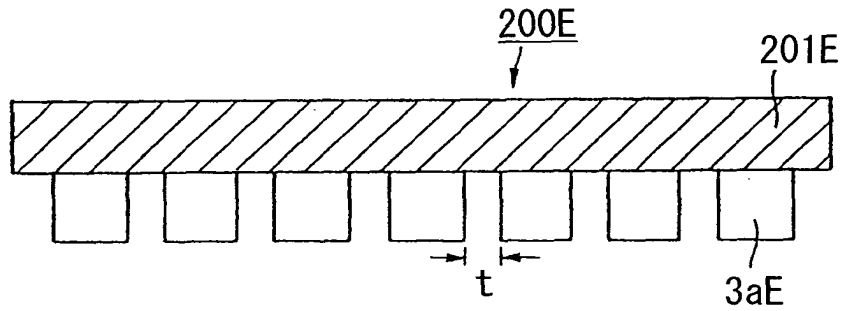
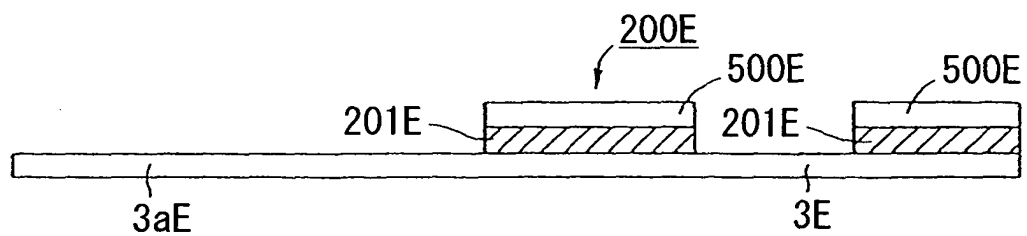


FIG. 26



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FIG. 27

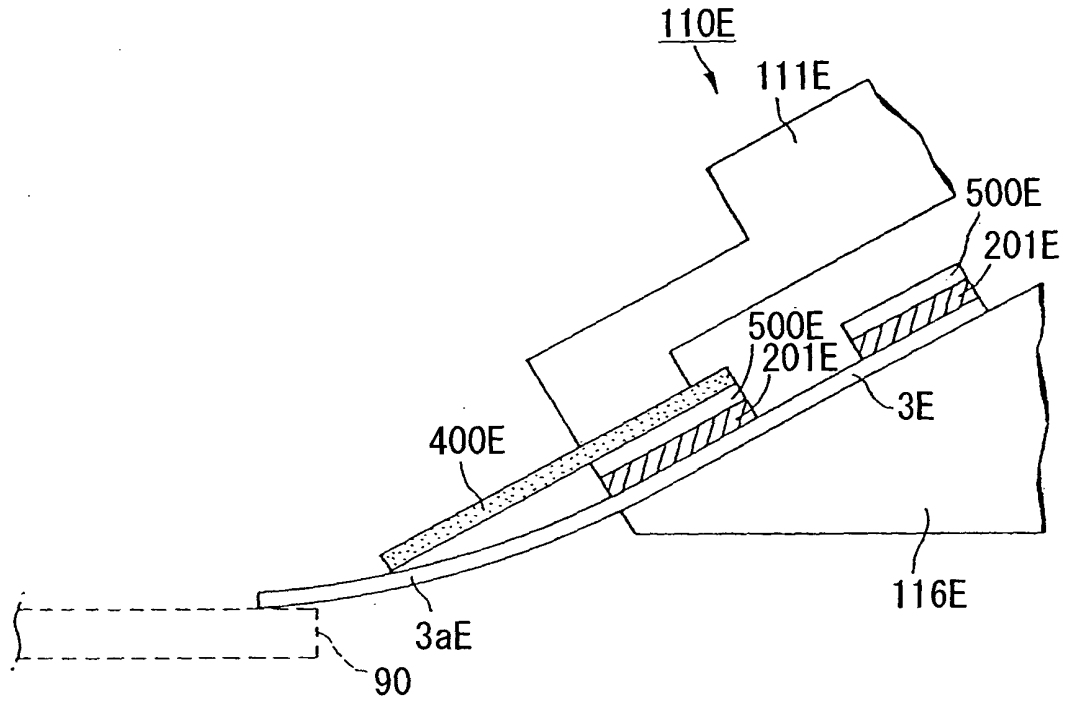


FIG. 28

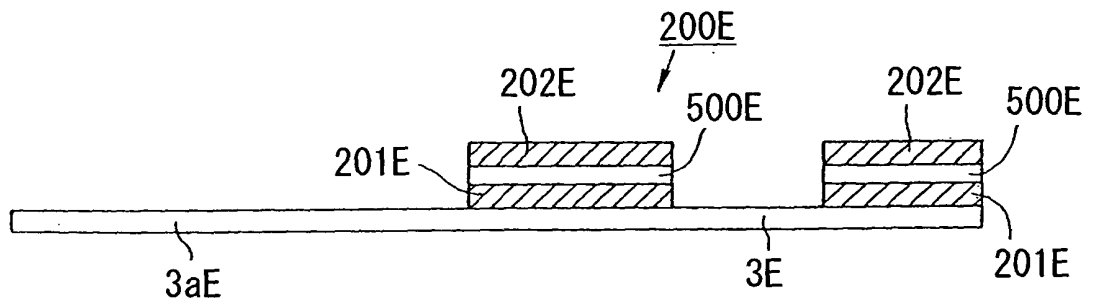


FIG.29

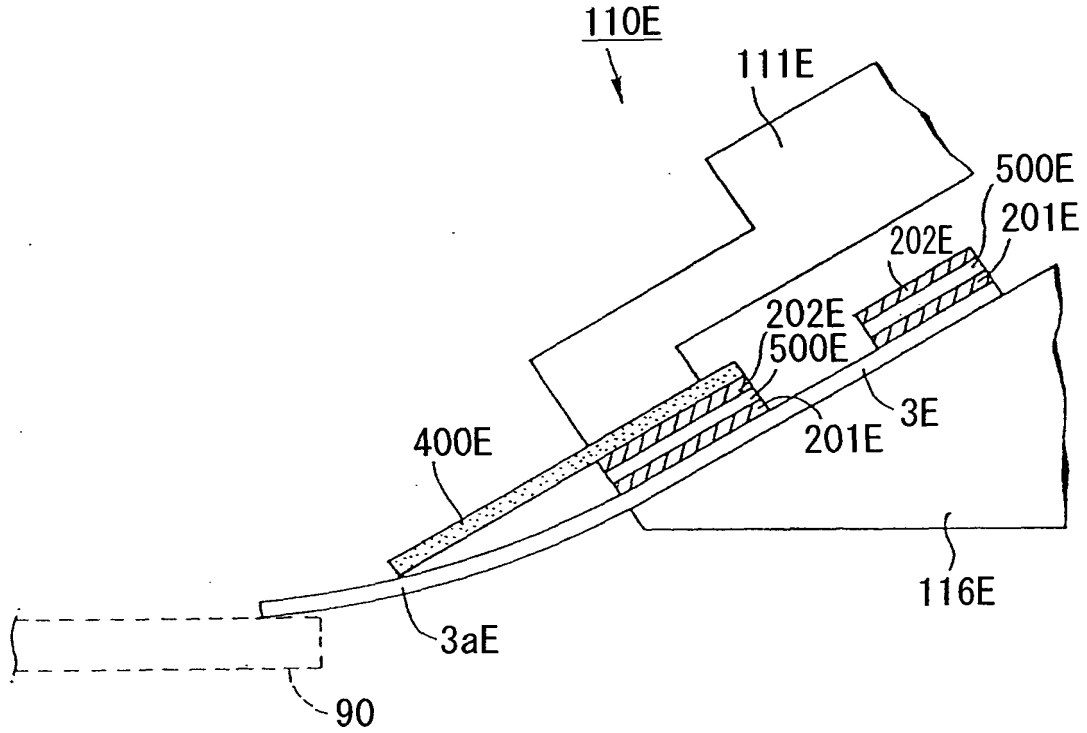


FIG. 30

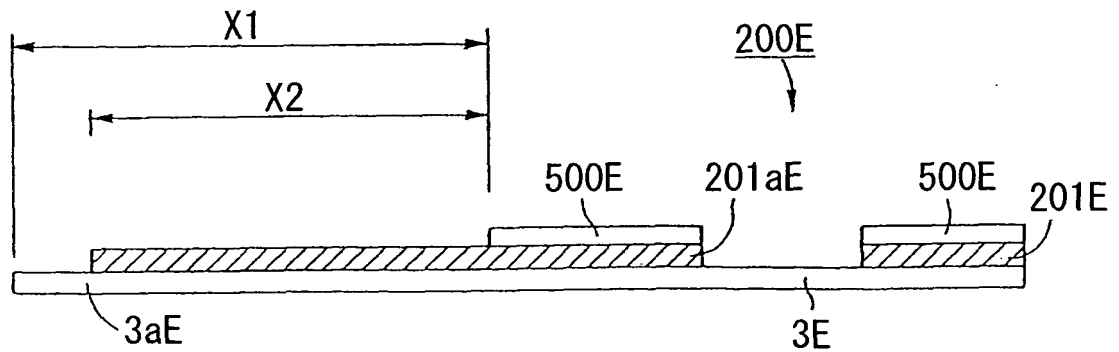


Diagram 200E is a cross-sectional view of a semiconductor device. It shows a substrate 3E with a layer 3aE on its top surface. Two regions, 201aE and 202E, are formed on the substrate 3E, separated by a gap 500E. The regions 201aE and 202E are shown as hatched areas. Dimensions X1 and X2 are indicated for the regions 201aE and 202E, respectively.

FIG. 33

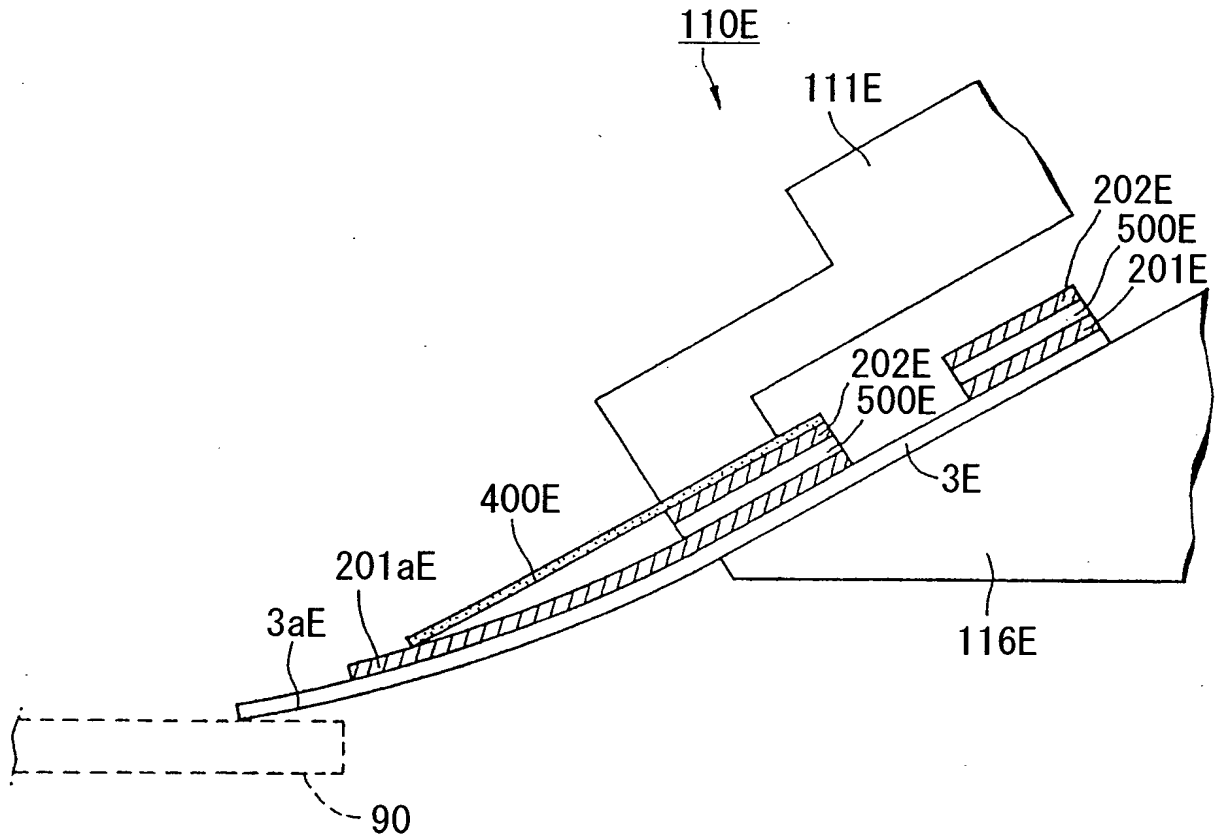


FIG. 34

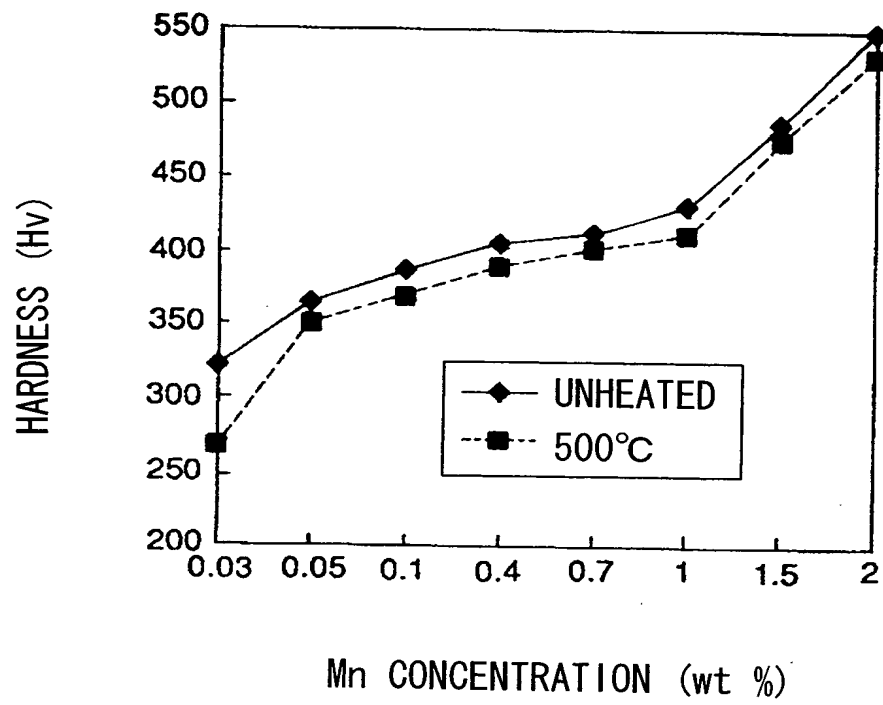
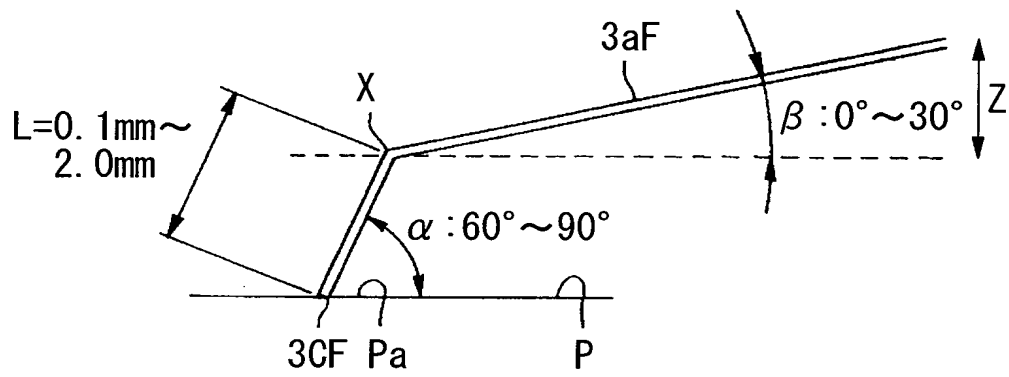
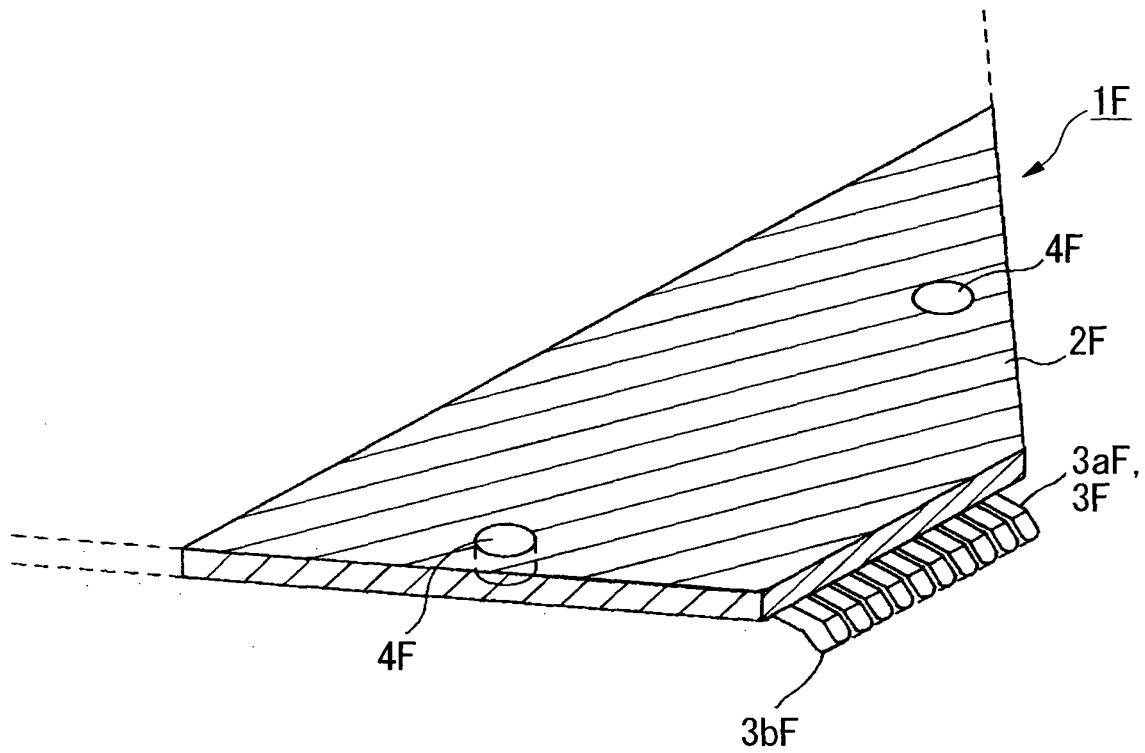


FIG. 35



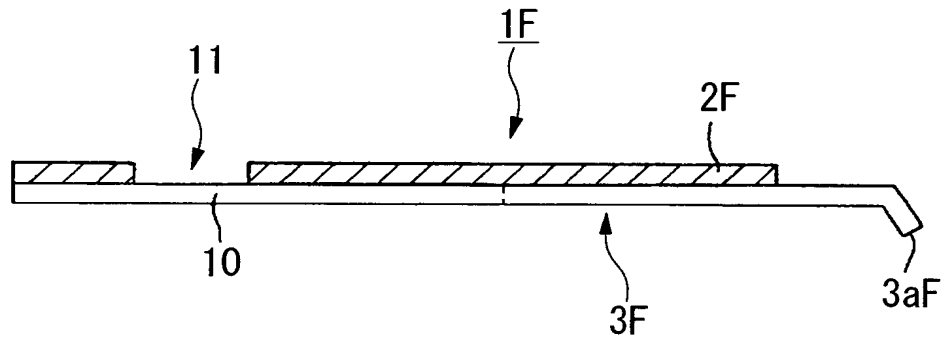
10076508-061902

FIG. 36



10076508-061902

FIG. 37



10076508-061902

FIG. 39

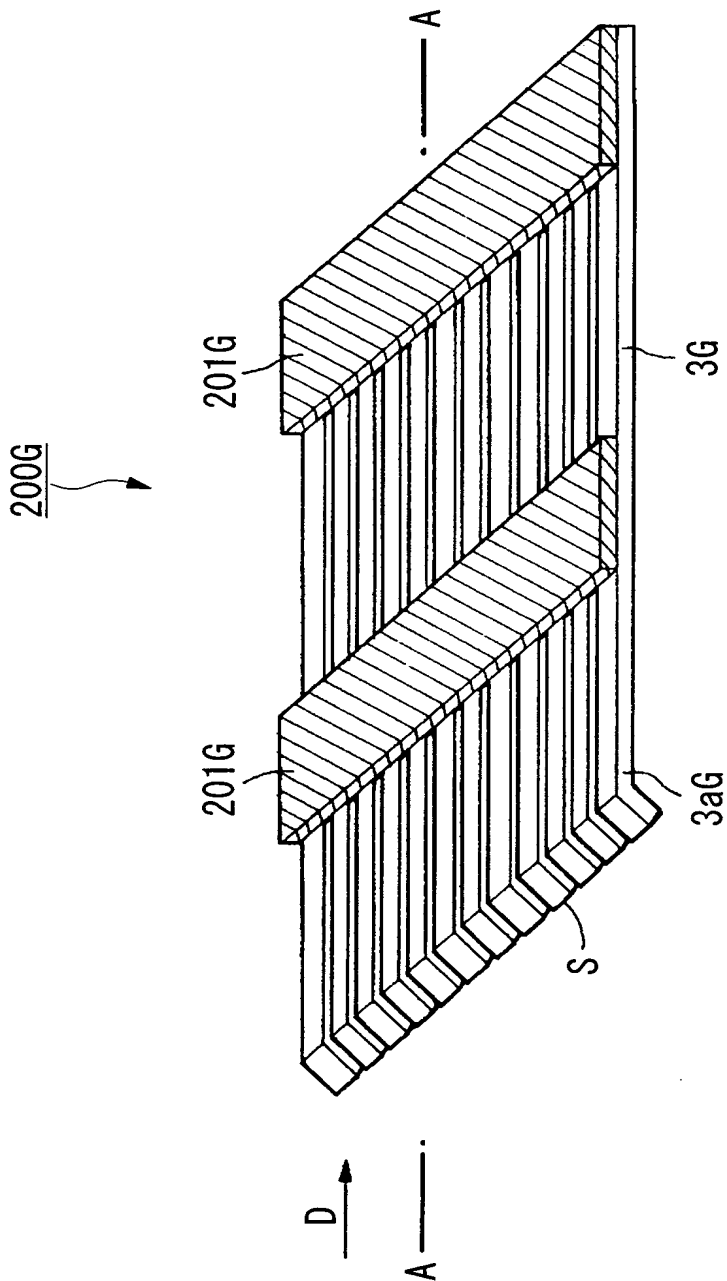
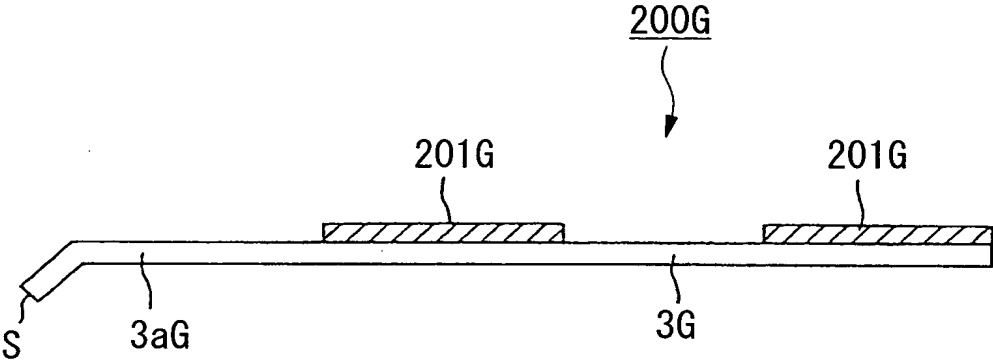


FIG. 40



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FIG. 41

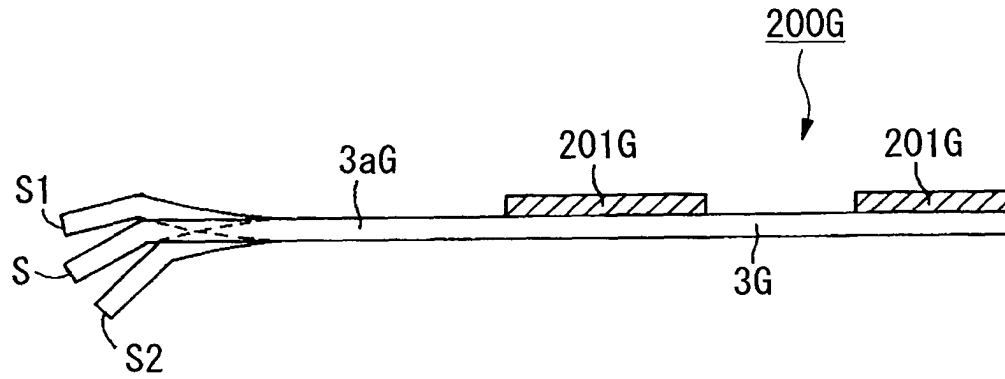


FIG. 42

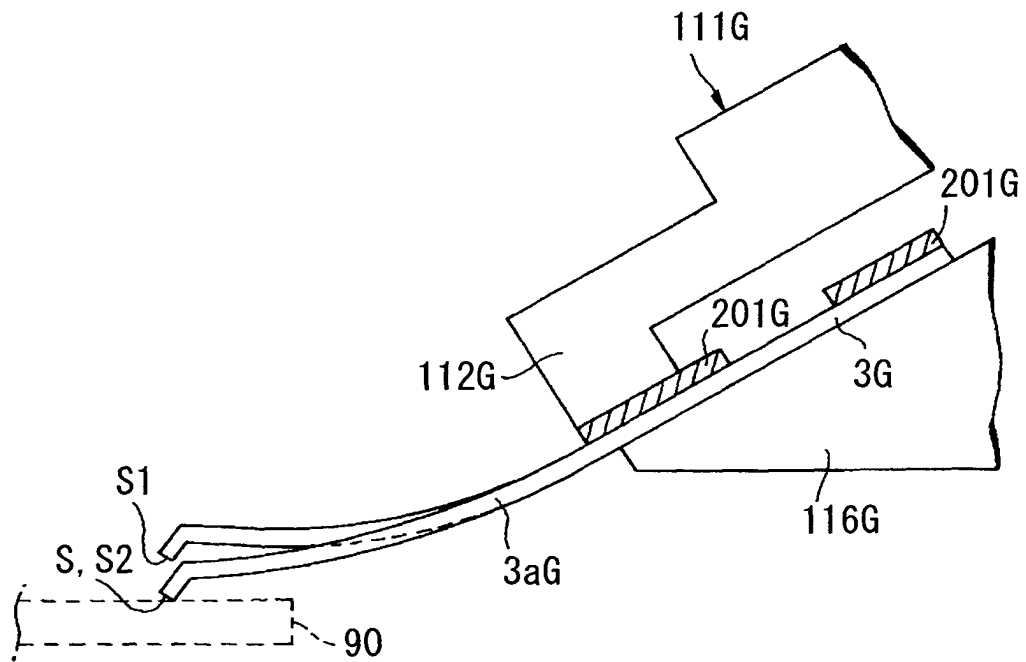
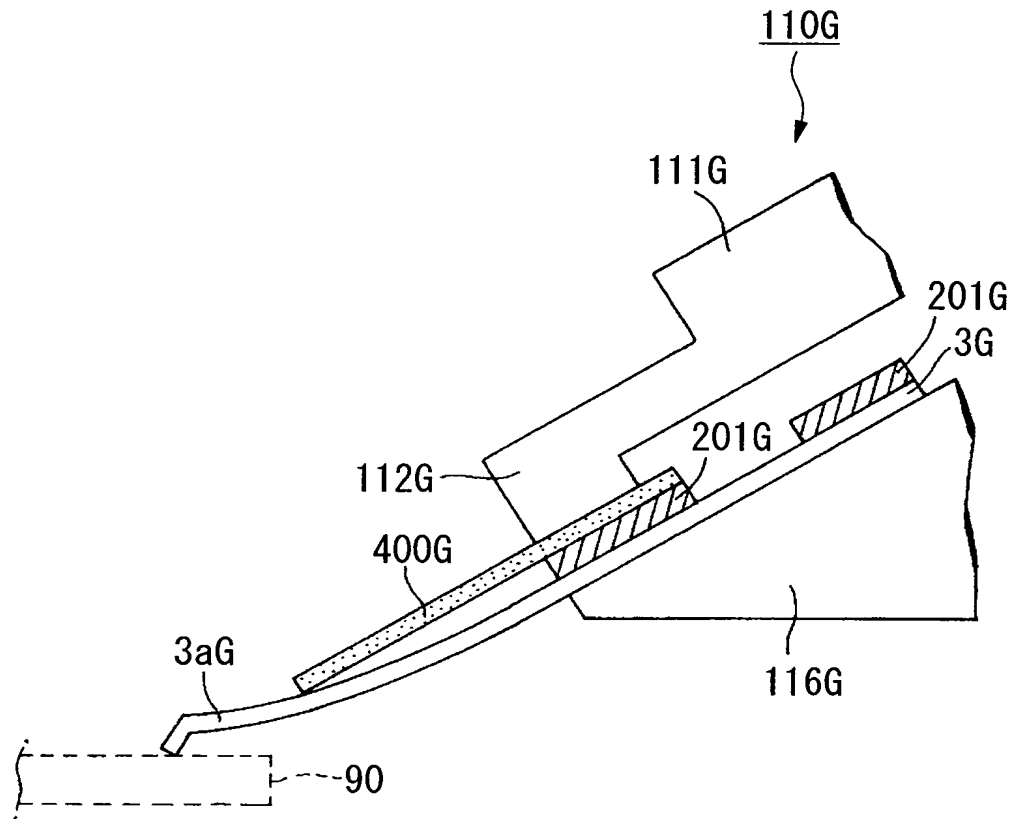


FIG. 43



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FIG. 44

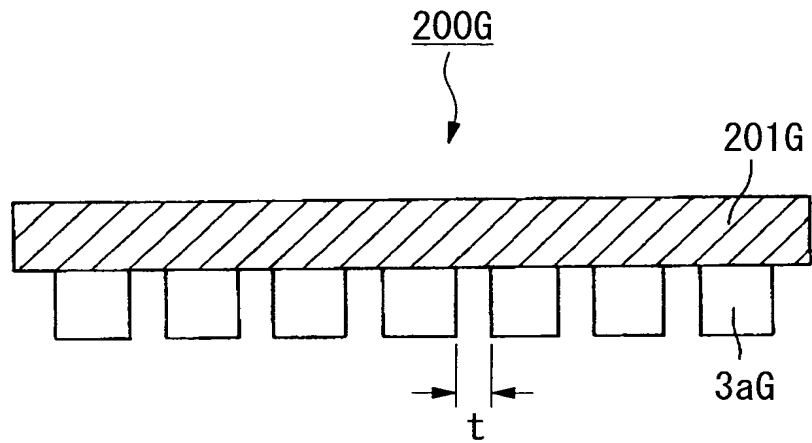


FIG. 45

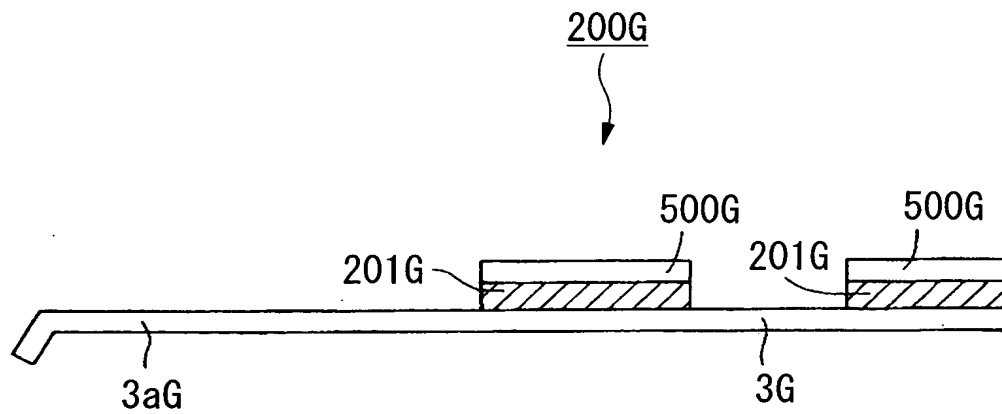


FIG. 46

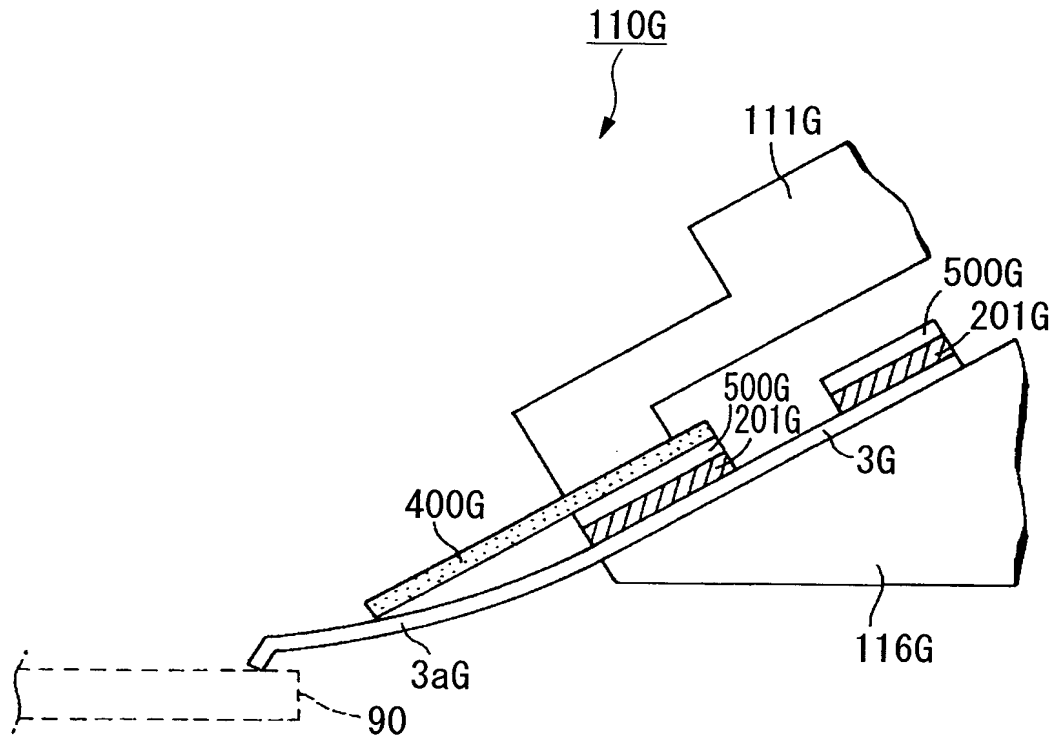
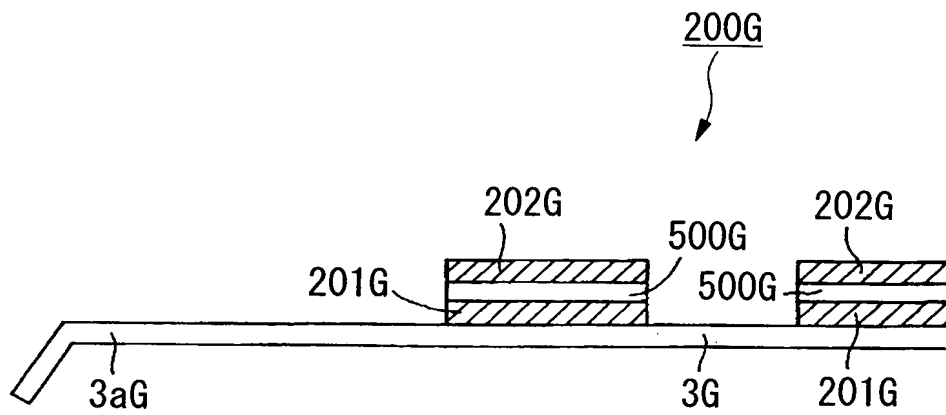


FIG. 47



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FIG. 48

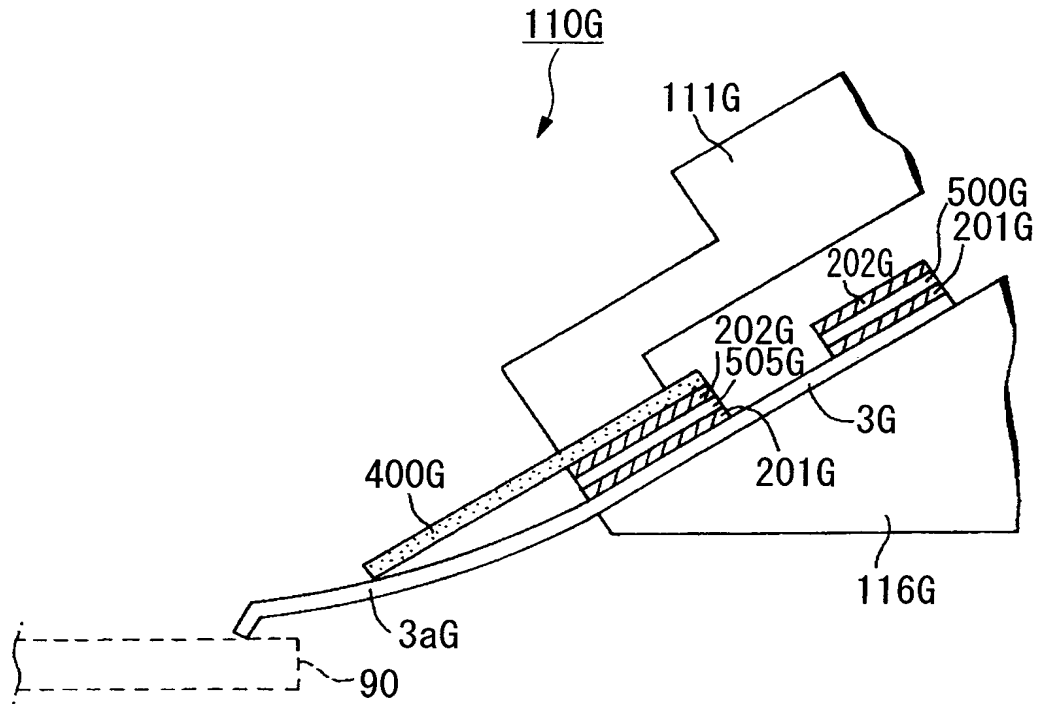


FIG. 49

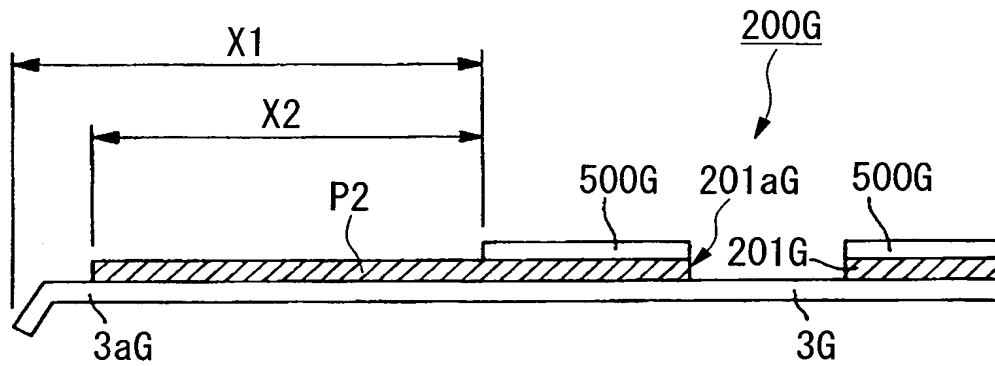


FIG. 50

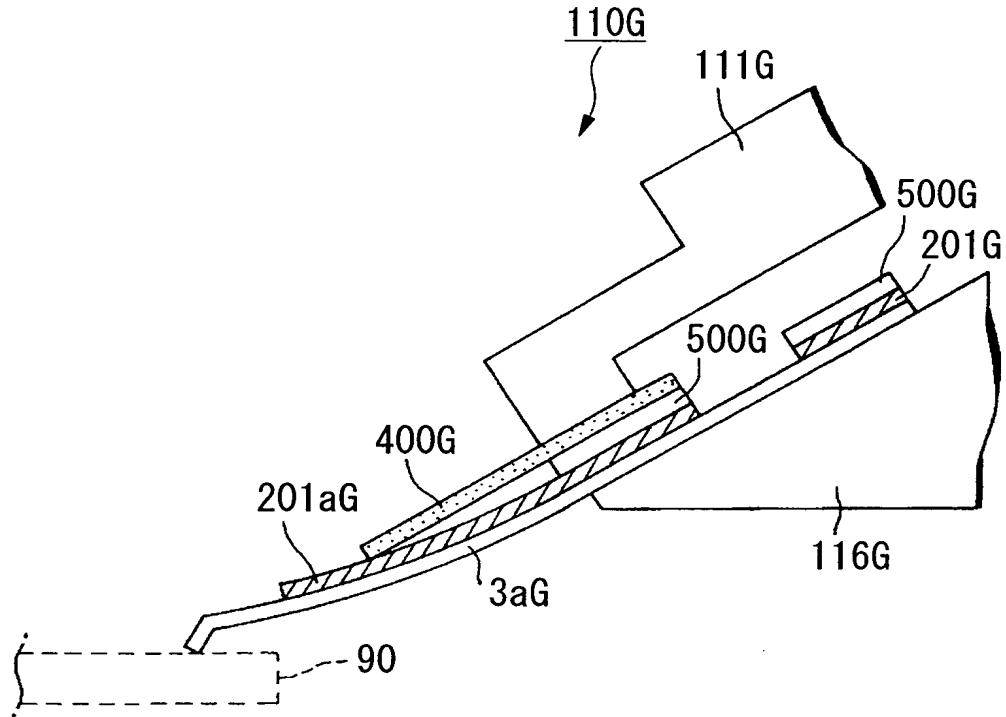
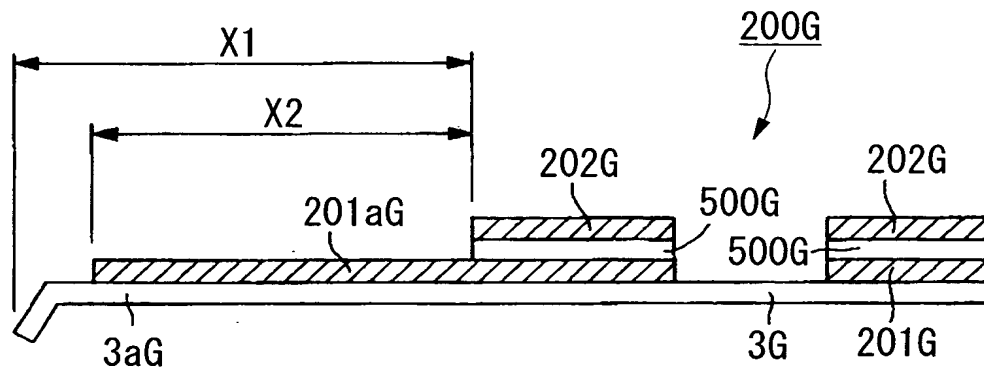
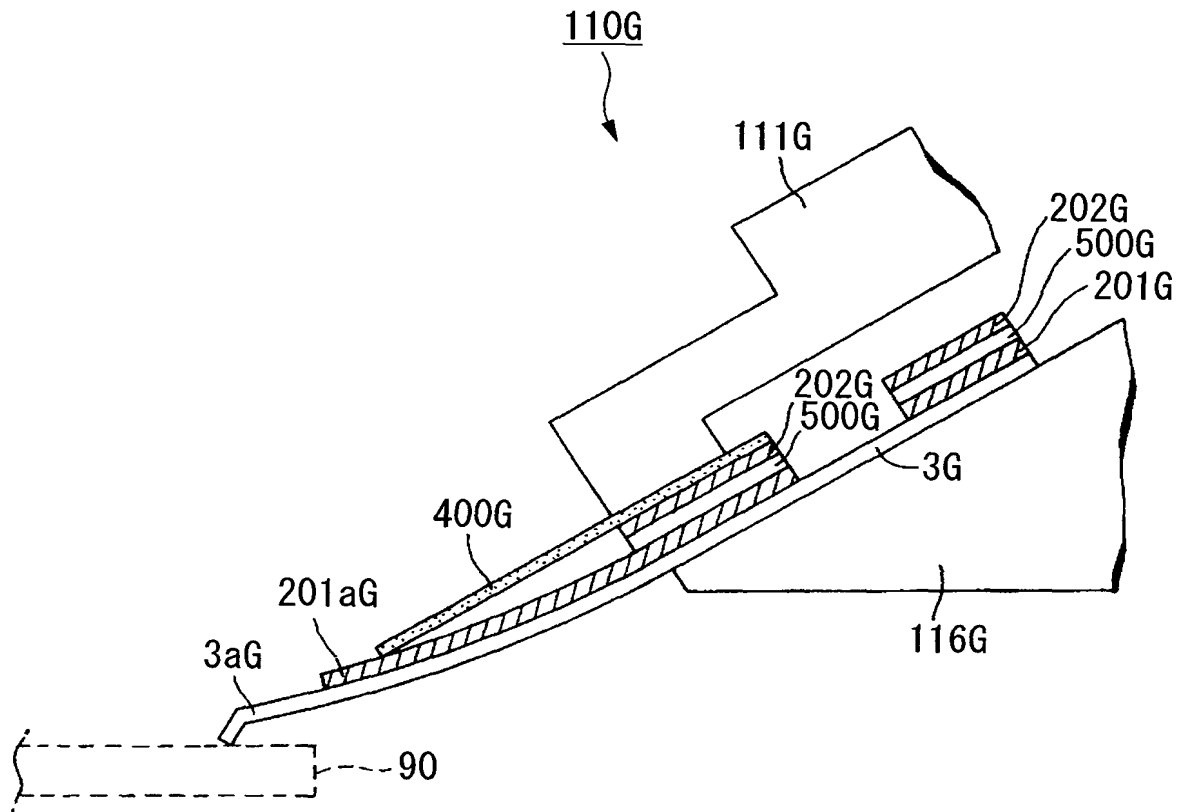


FIG. 51



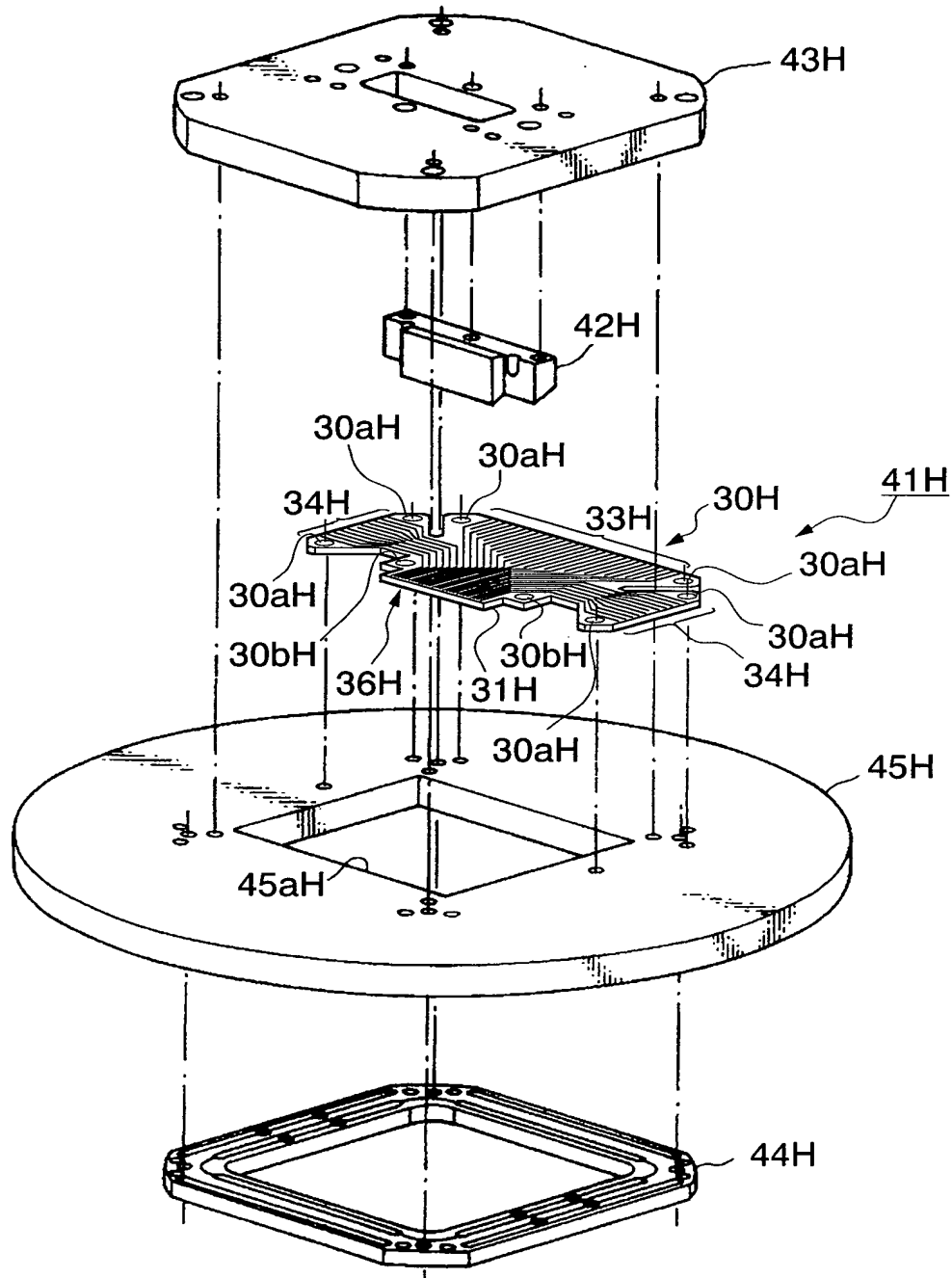
10076508-061902

FIG. 52



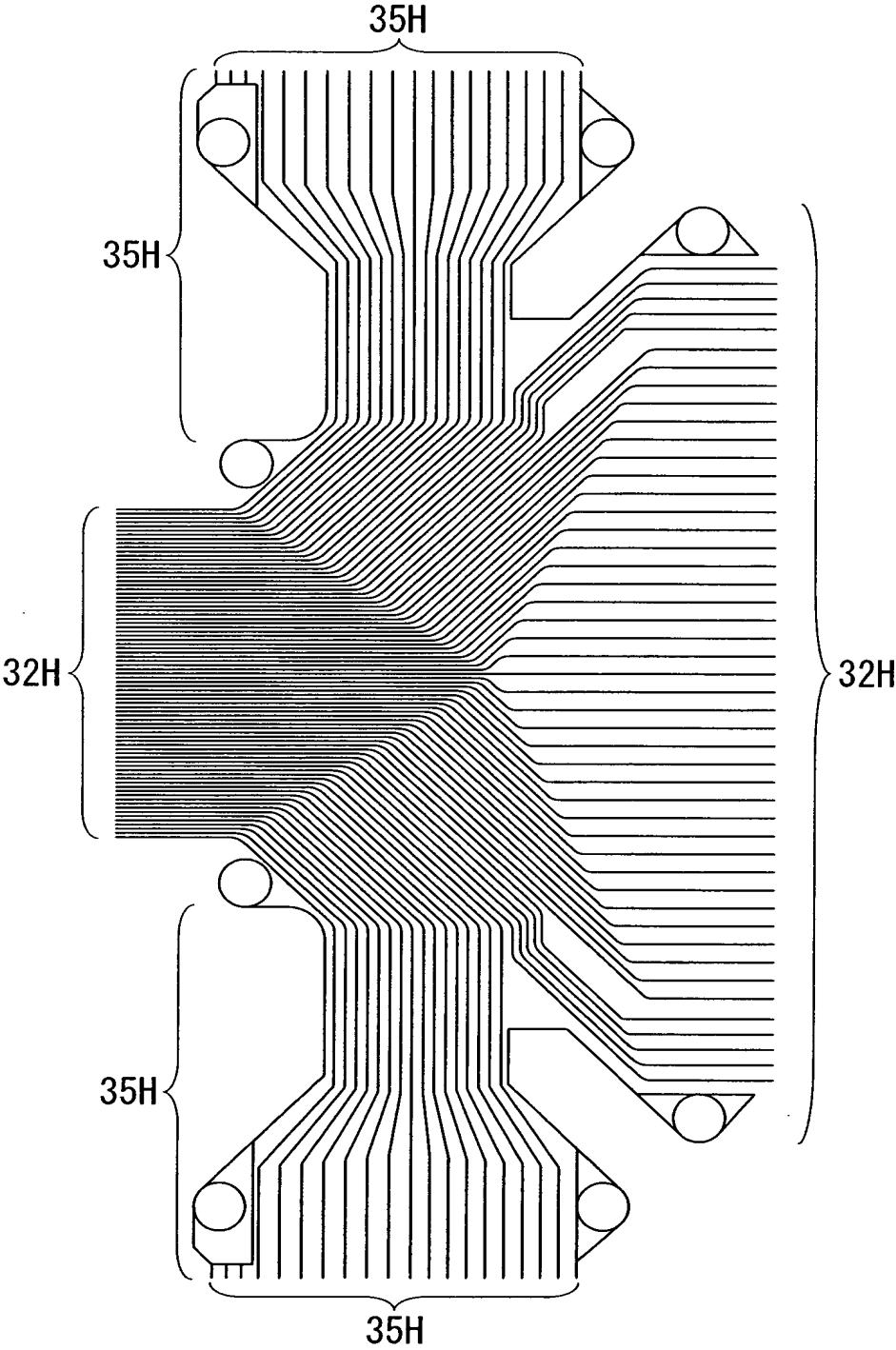
1006508-061900

FIG. 53



205190" 2059/001

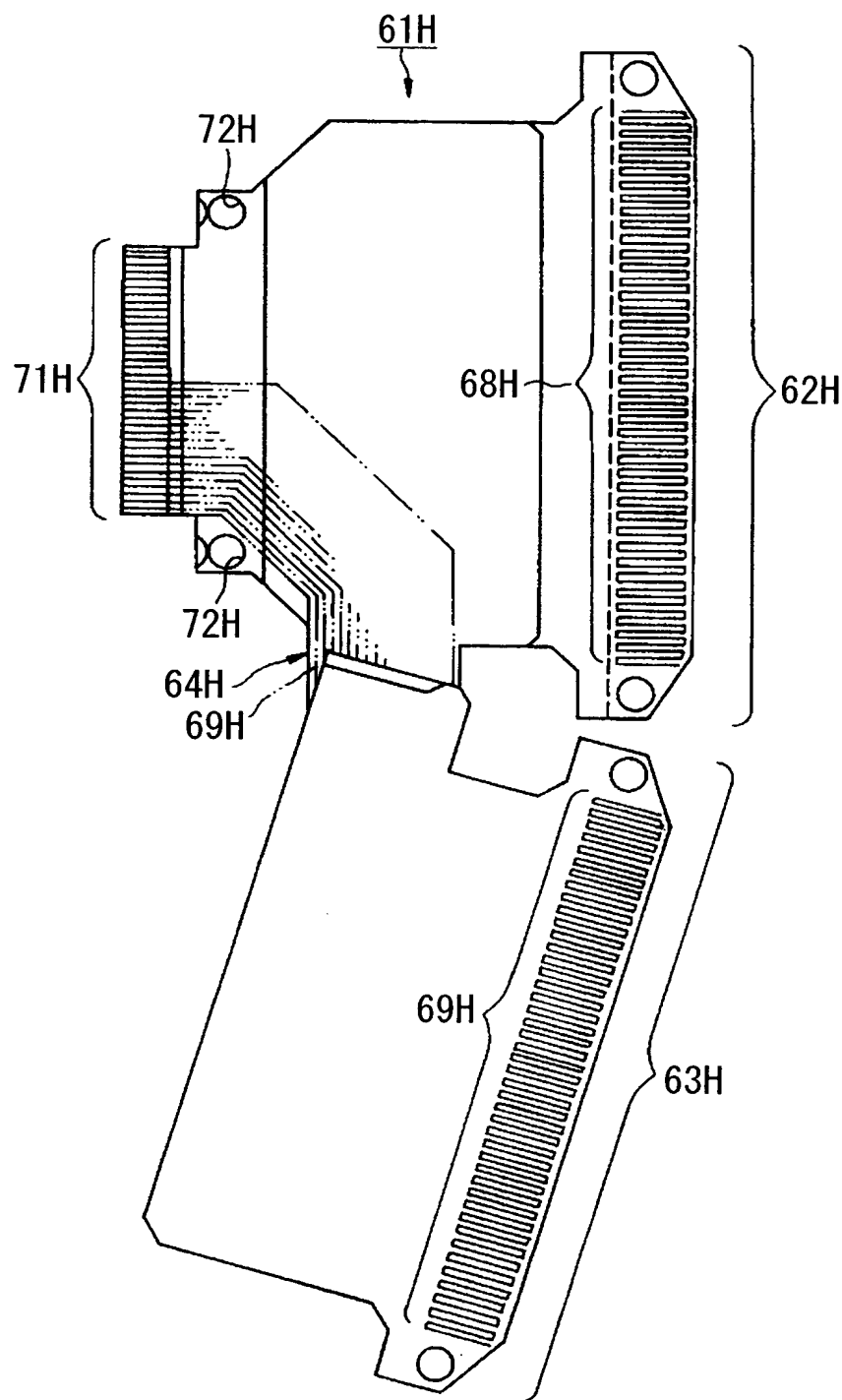
FIG. 54



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A cross-sectional view of a semiconductor device. It shows a central rectangular layer labeled 'I' positioned on a substrate labeled 'T'. Above the central layer, there are several wavy, finger-like structures extending upwards, collectively labeled '50H'. On the left side, a label '51H' points to the base of these structures. On the right side, a label '52H' points to one of the wavy fingers. Further up and towards the center, labels '53H' and '54H' point to specific parts of the upper layers. At the very top, two small protrusions are labeled '55H'. To the far right, a label '45H' points to the outer boundary or another part of the device structure.

FIG. 56



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A cross-sectional view of a semiconductor device 60H. The device features a substrate 66H with a top layer 62H. A gate structure 68H is formed on the top layer 62H, with a gate oxide 69H and a gate electrode 65aH. A source/drain region 64H is formed in the substrate 66H, with a source/drain oxide 63H. A contact pad 67H is formed on the source/drain region 64H. A passivation layer 70H is formed on the top surface of the device. A side wall 71H is formed on the side of the gate structure 68H, and a side wall 72H is formed on the side of the source/drain region 64H. A contact pad 73H is formed on the side wall 71H, and a contact pad 74H is formed on the side wall 72H.

FIG. 58

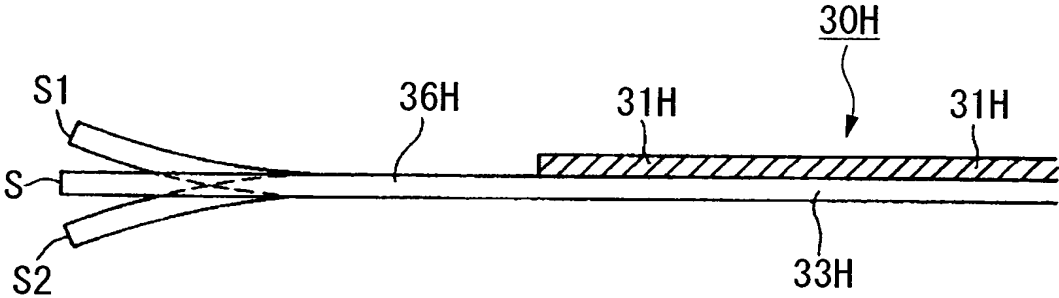
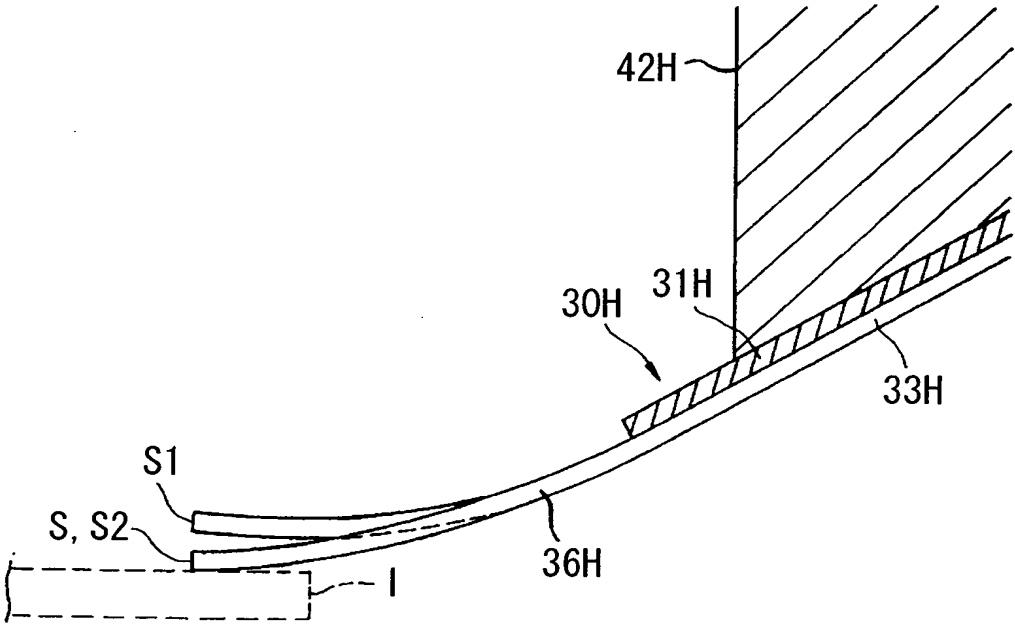


FIG. 59



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FIG. 60

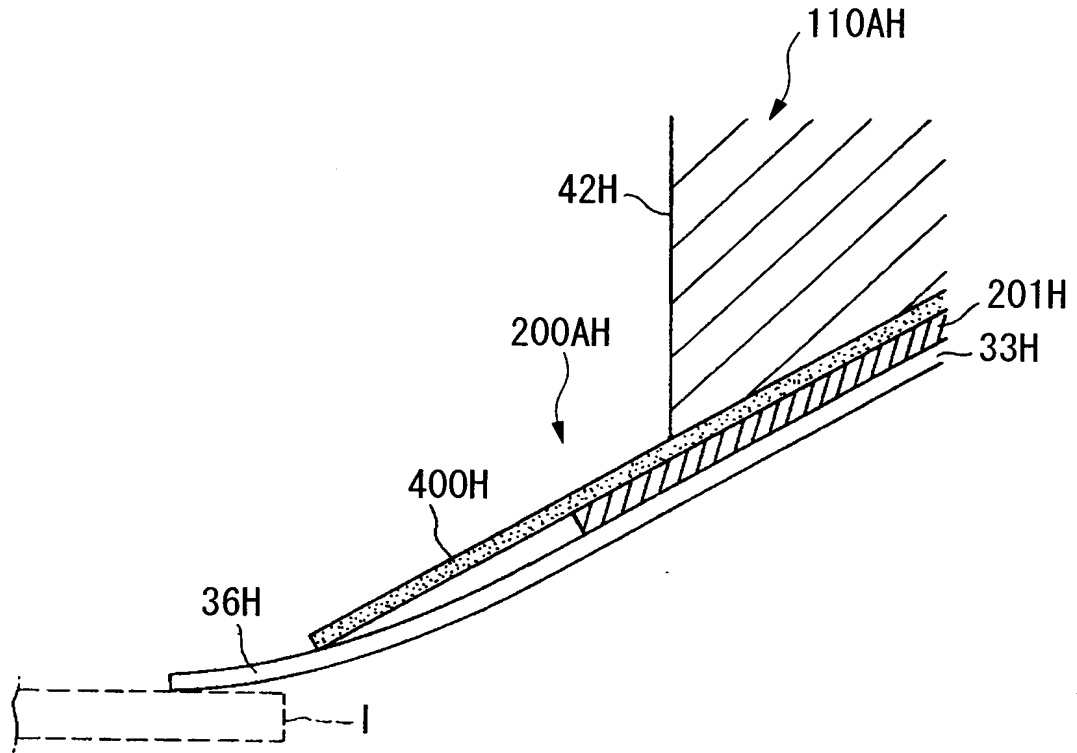
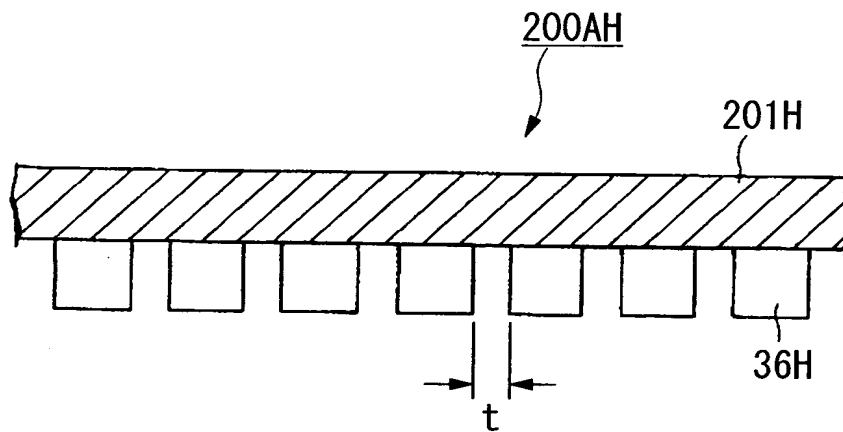


FIG. 61



206T90" 8059/00T

FIG. 62

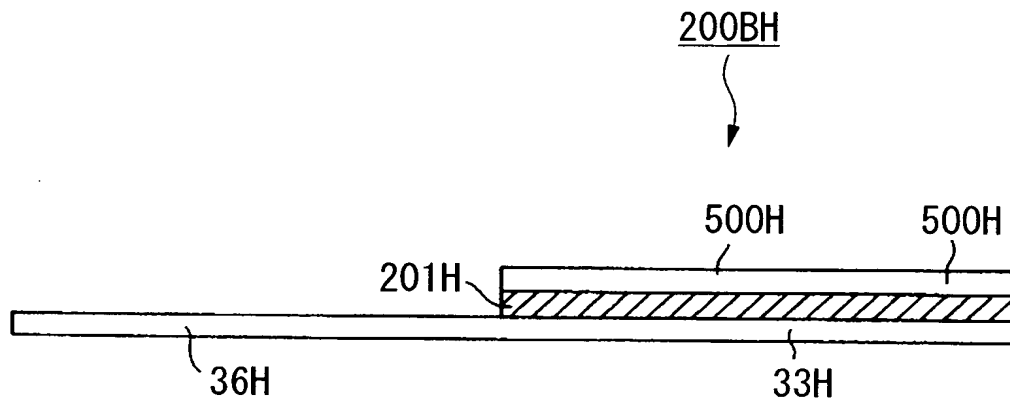
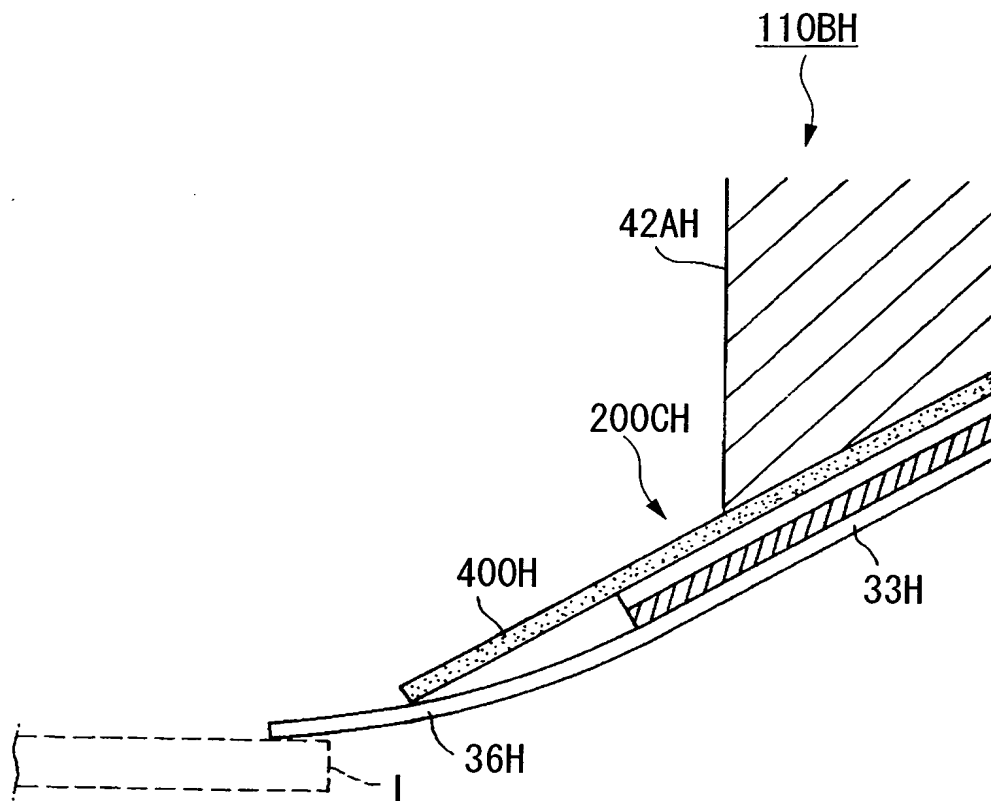


FIG. 63



206T90" 8059/00T

FIG. 64

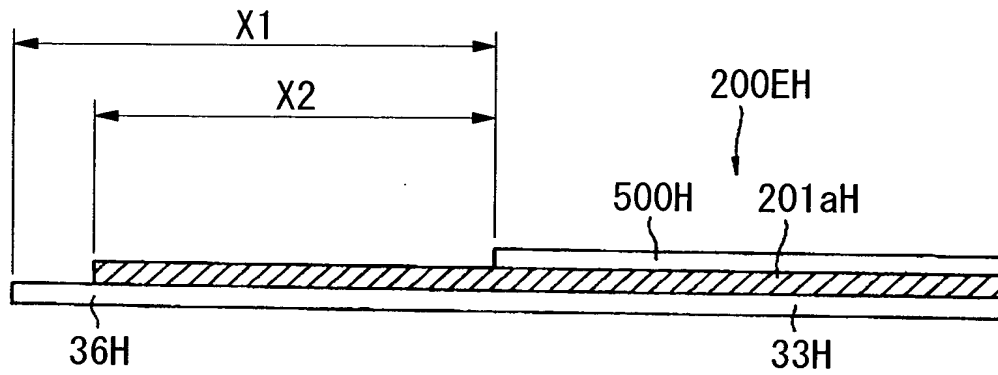


FIG. 65

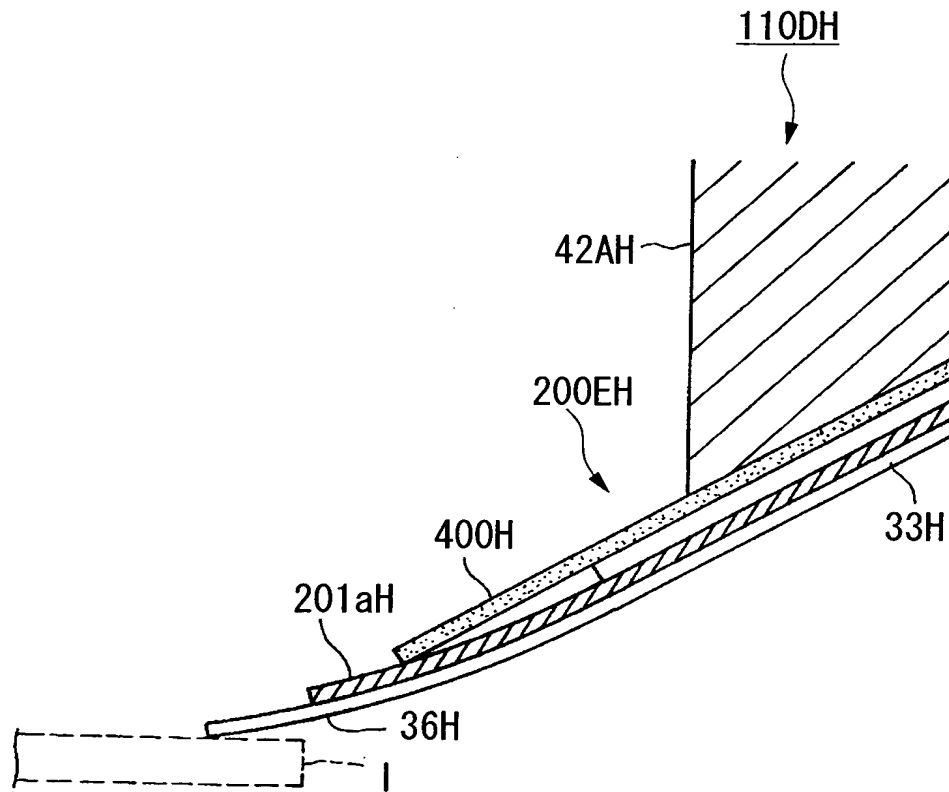
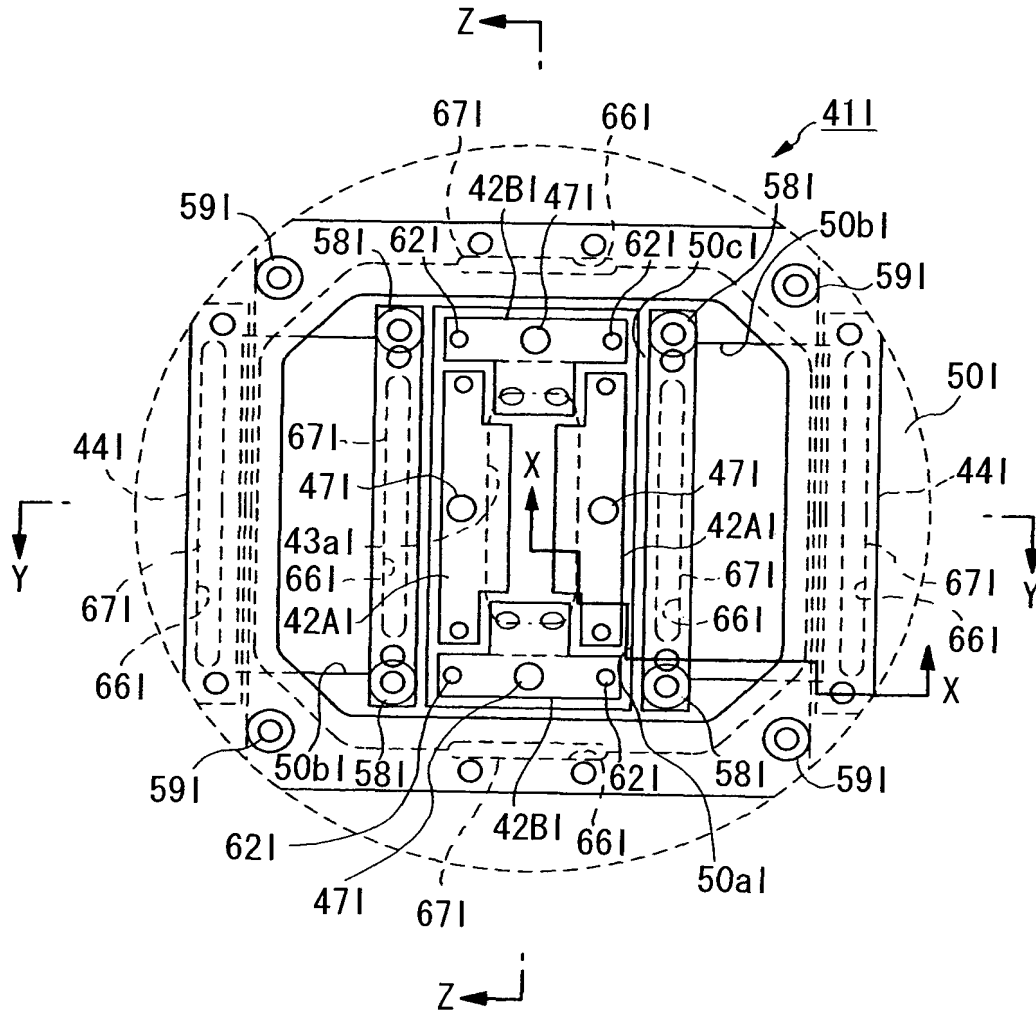


FIG. 66



10076508-061902

FIG. 67

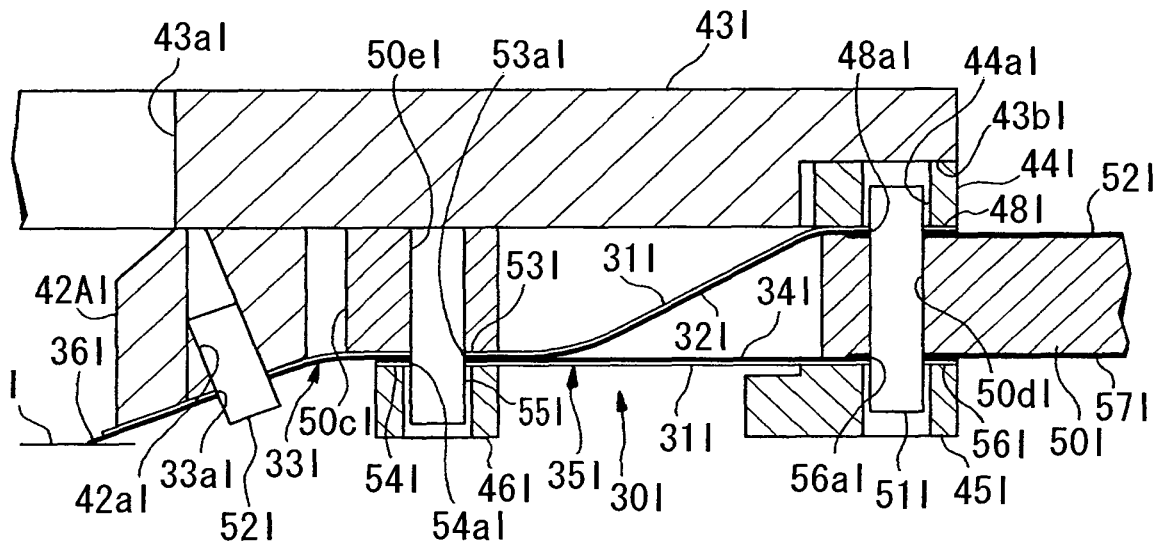


FIG. 68

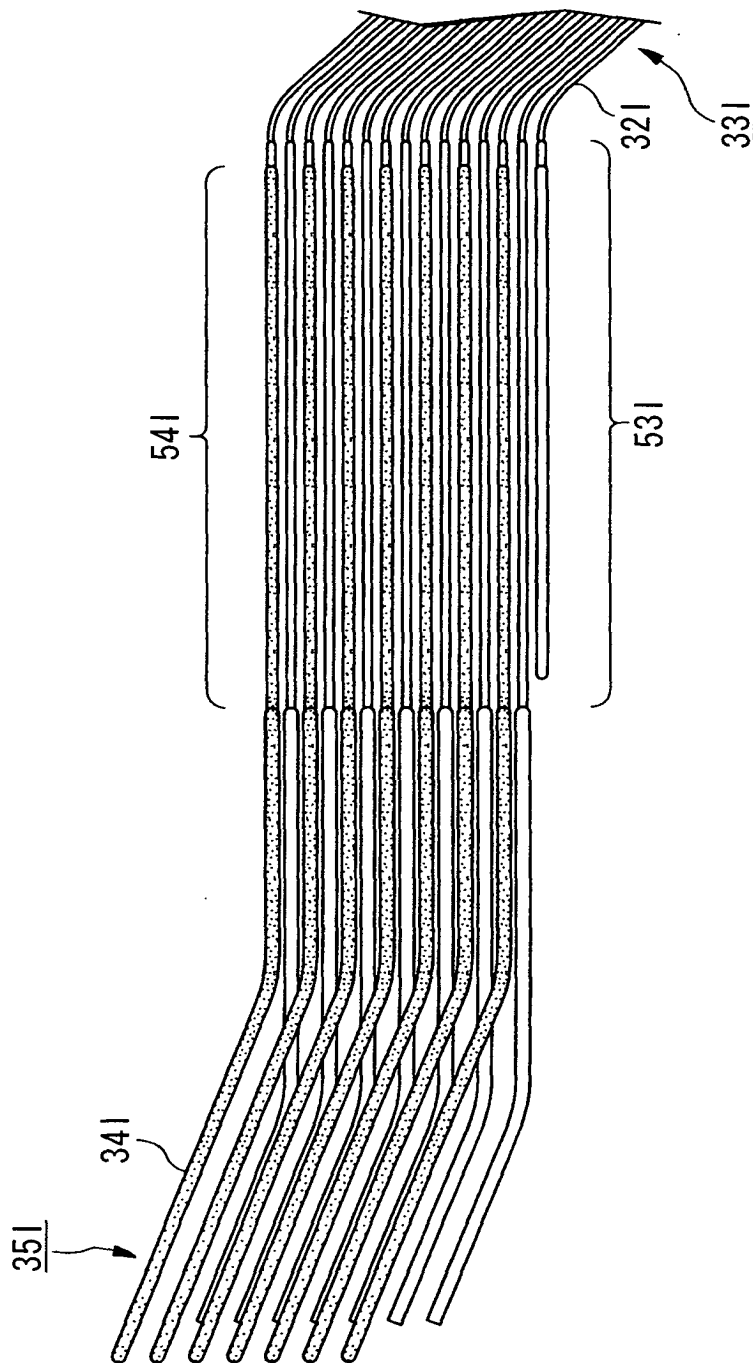
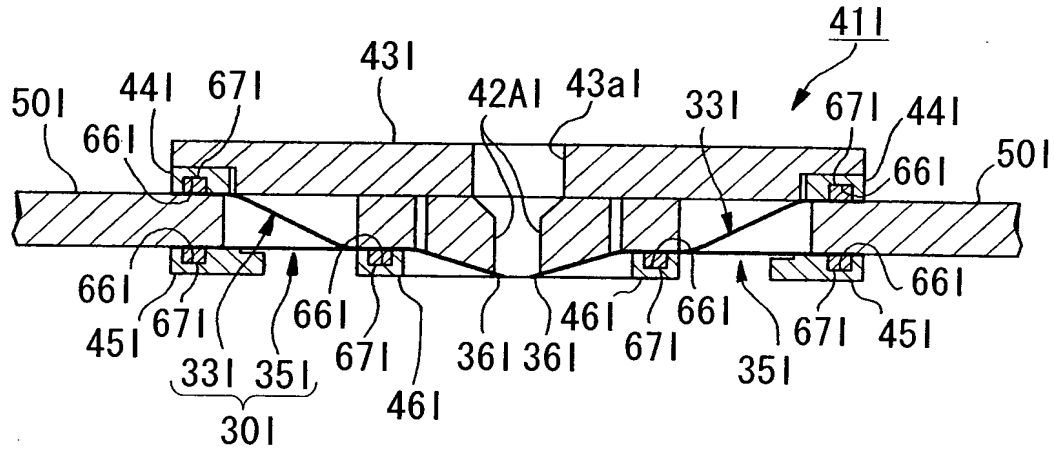
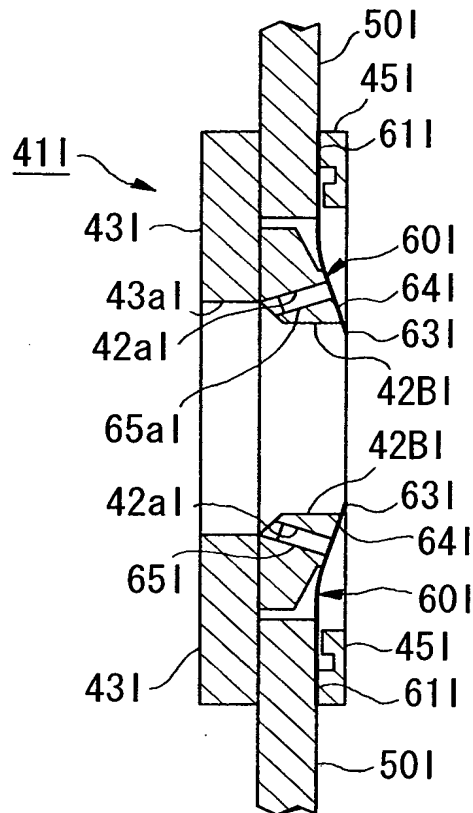


FIG. 69



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FIG. 70



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FIG. 71

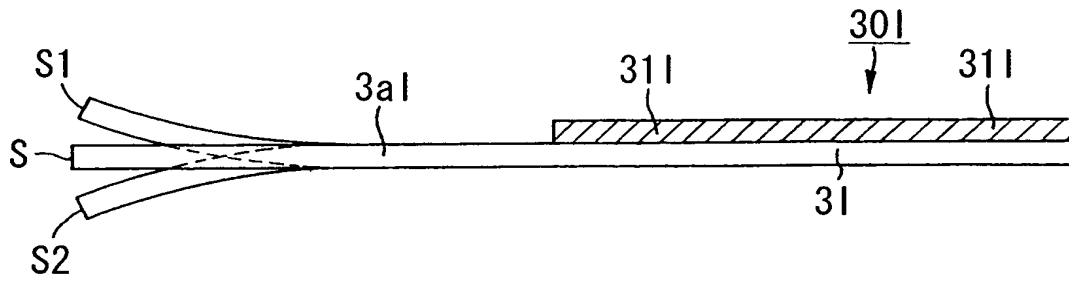
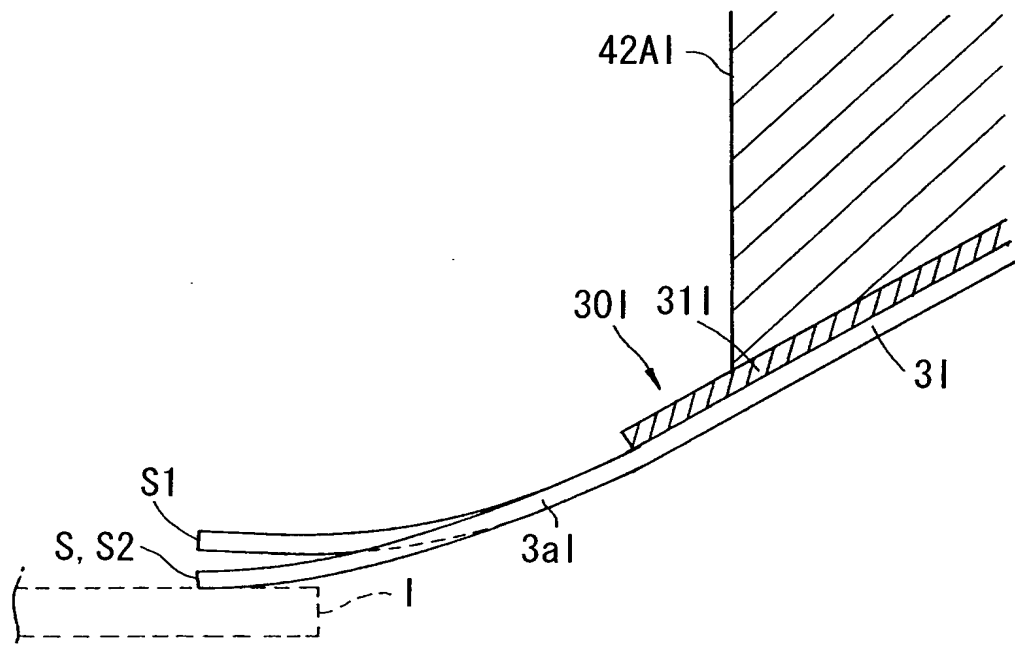


FIG. 72



206T90" 8059/00T

FIG. 73

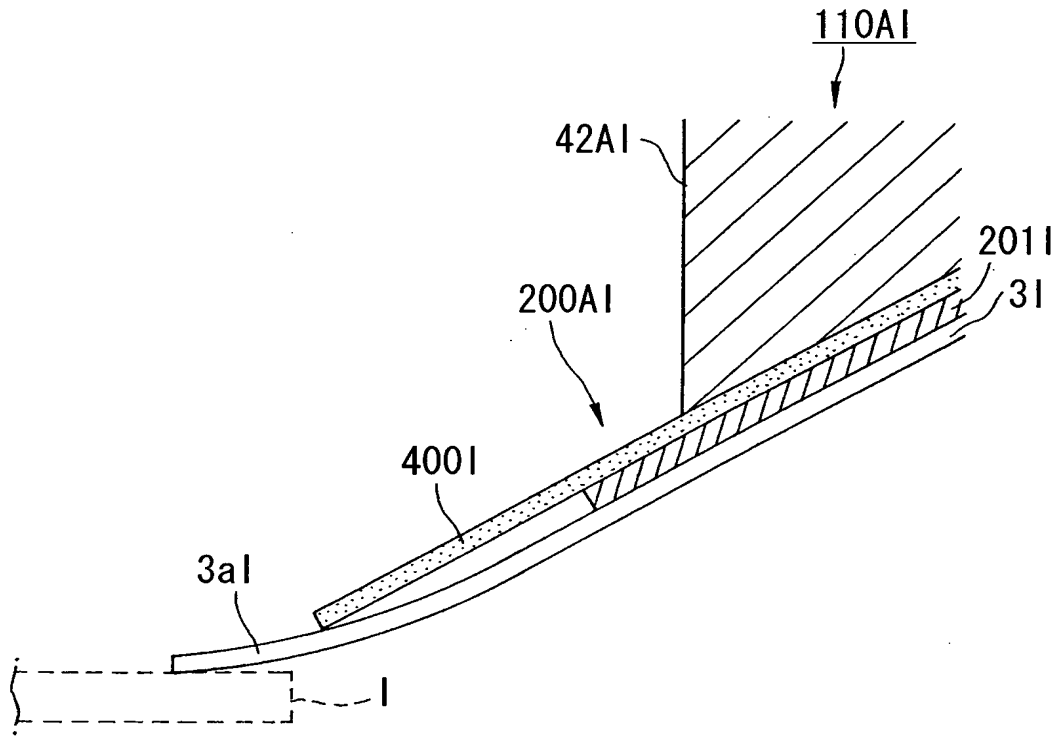


FIG. 74

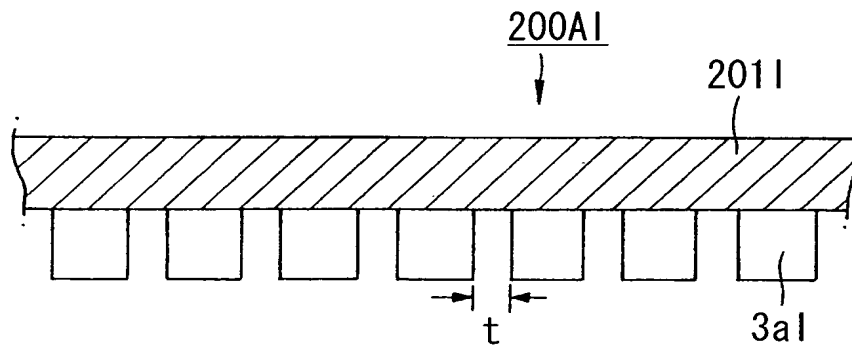


FIG. 75

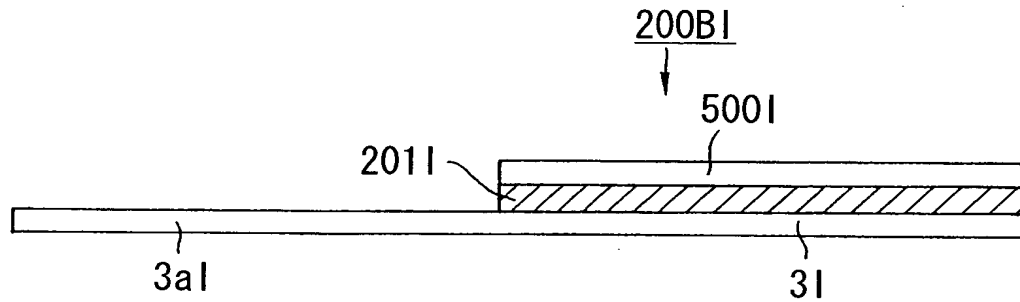


FIG. 76

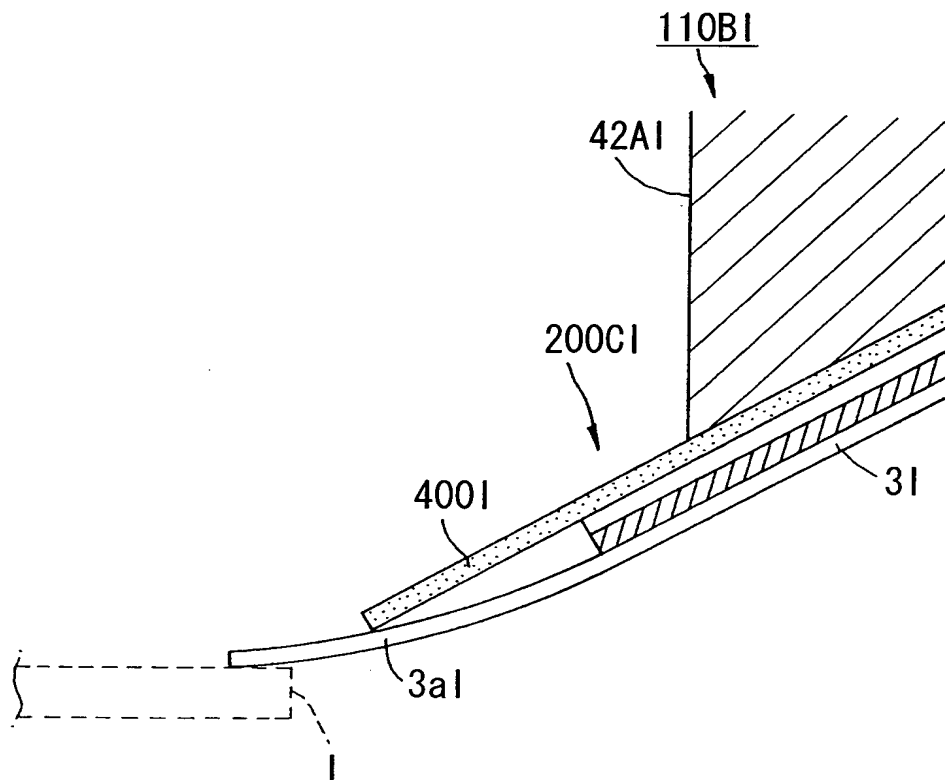


FIG. 77

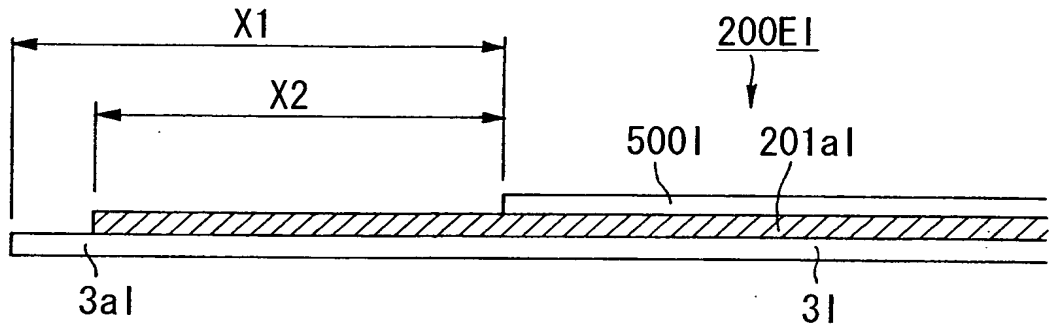
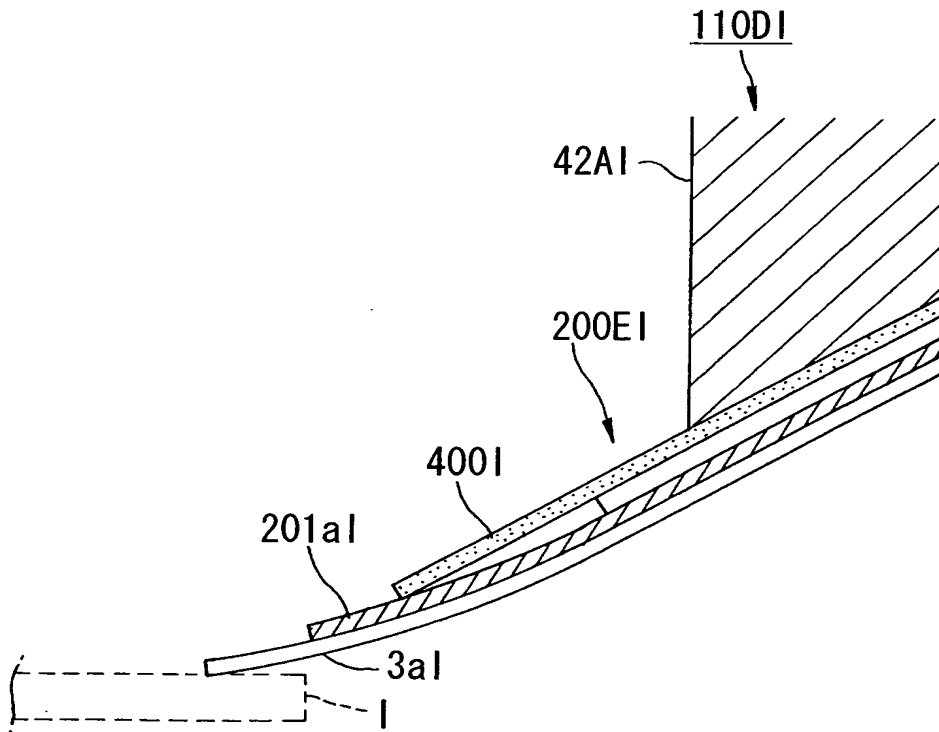


FIG. 78



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FIG. 79

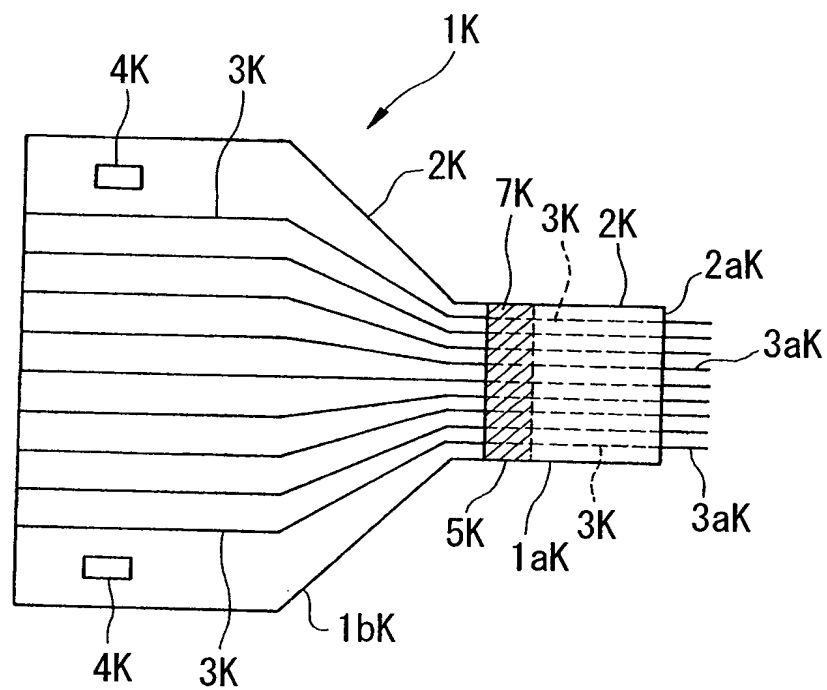


FIG. 80

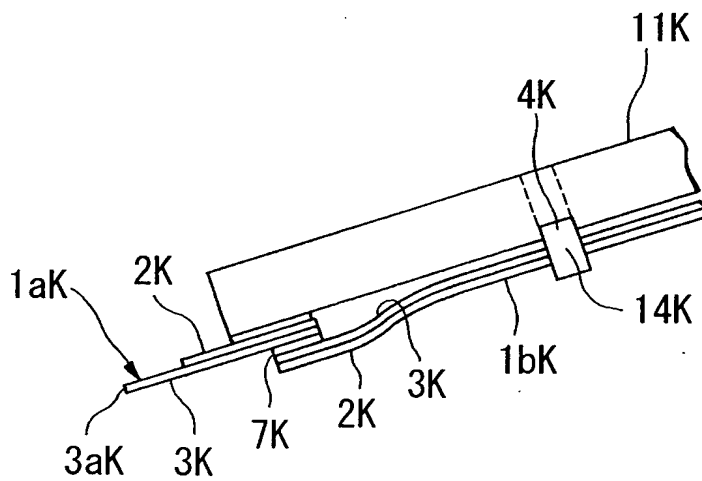


FIG. 81

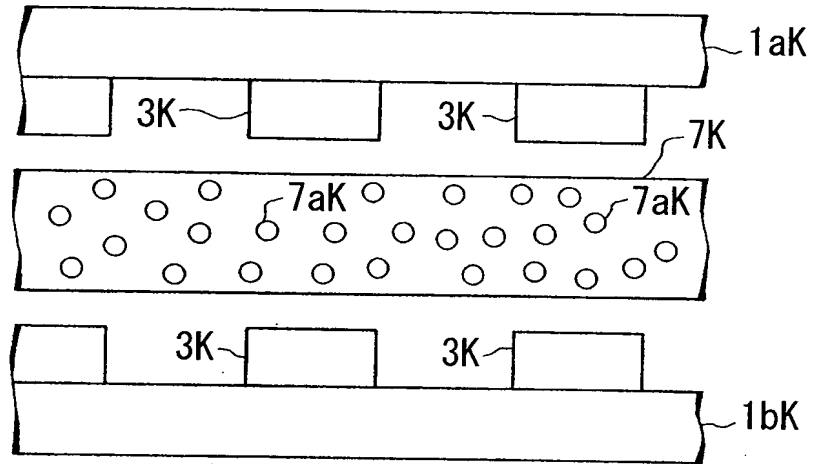
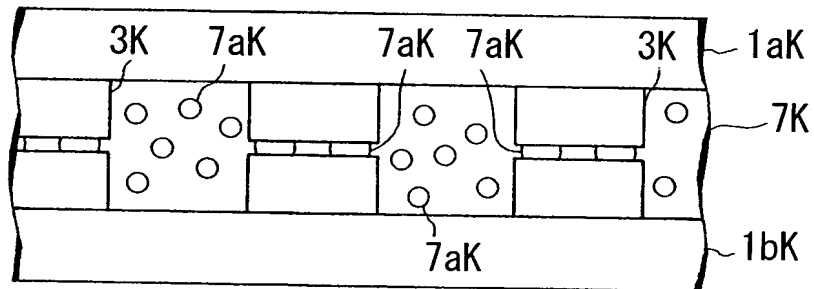


FIG. 82



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FIG. 83

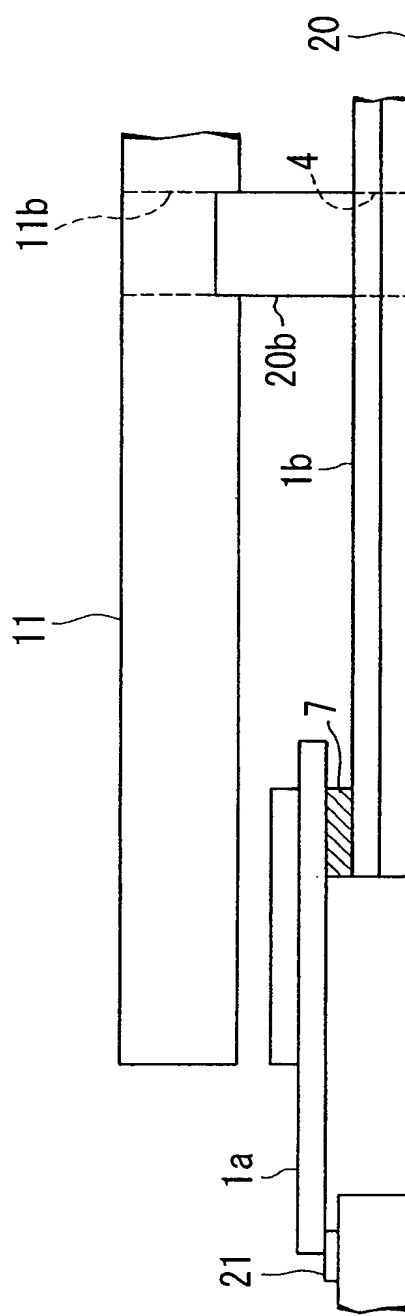
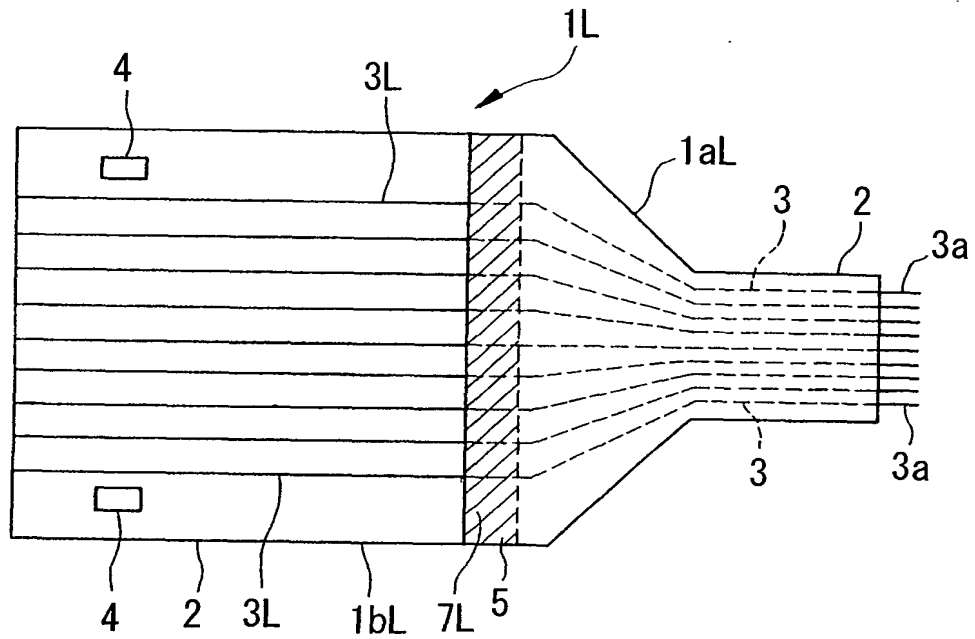


FIG. 84



10076508-05190T

FIG. 85

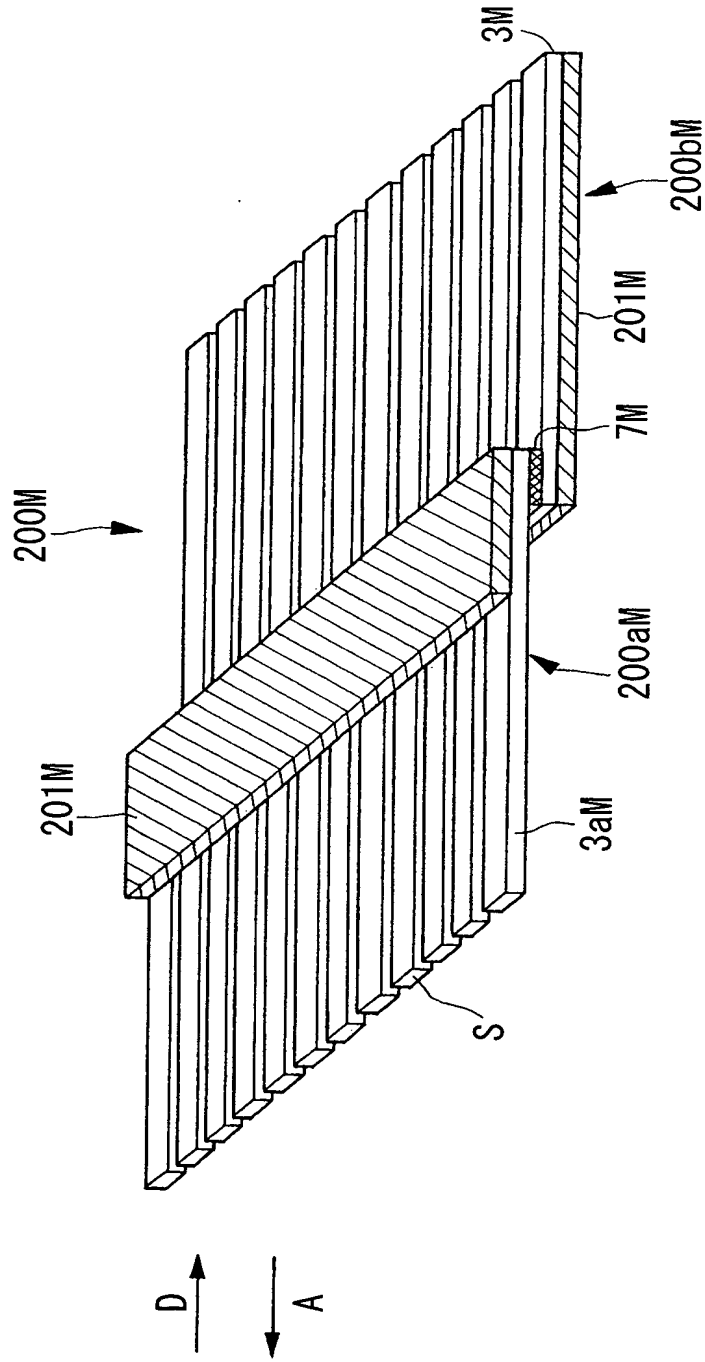
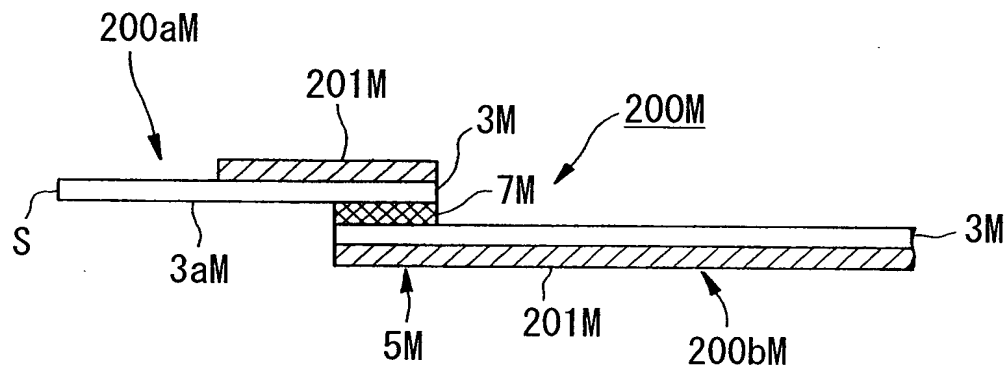


FIG. 86



10076508-061902

FIG. 88

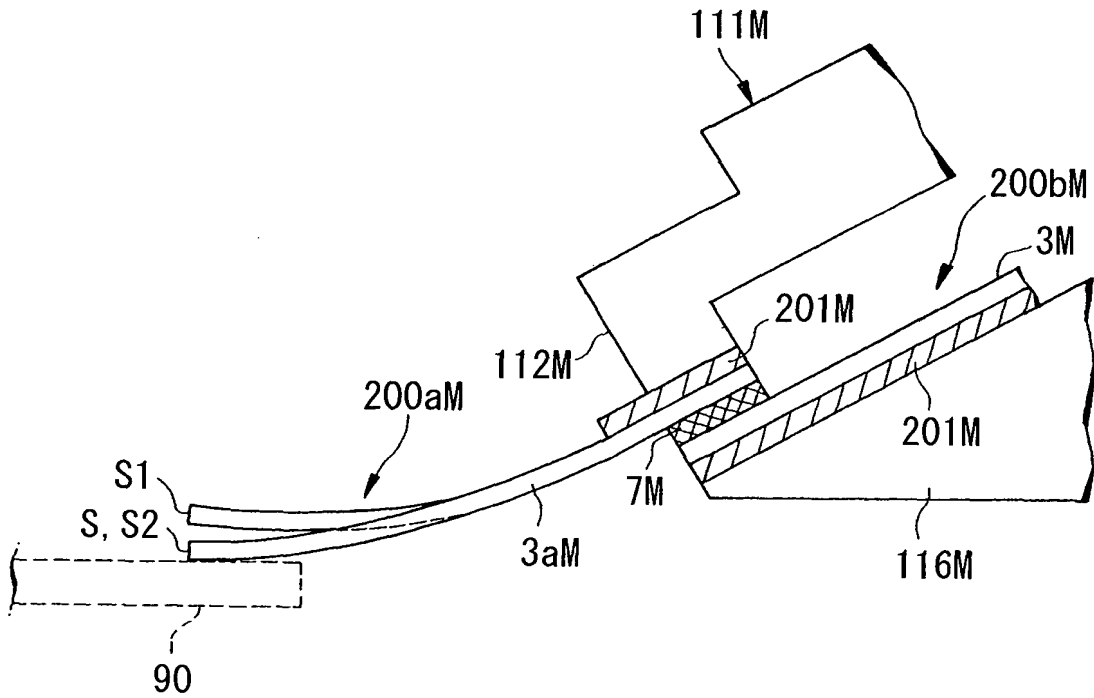
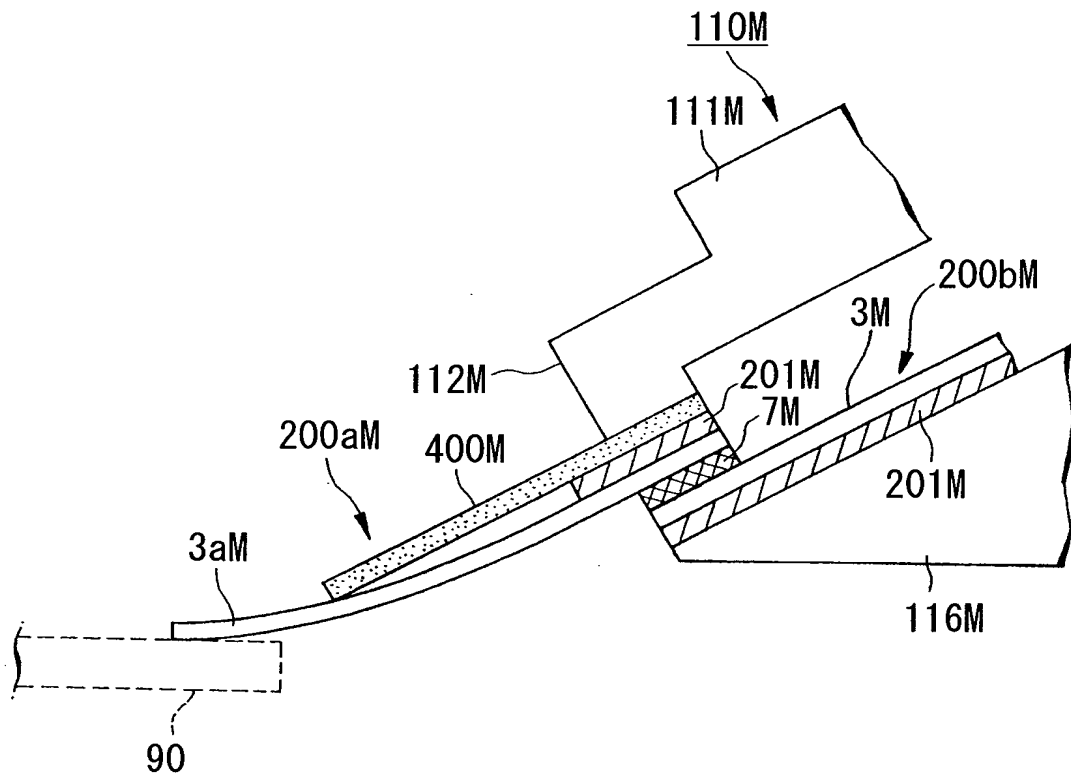
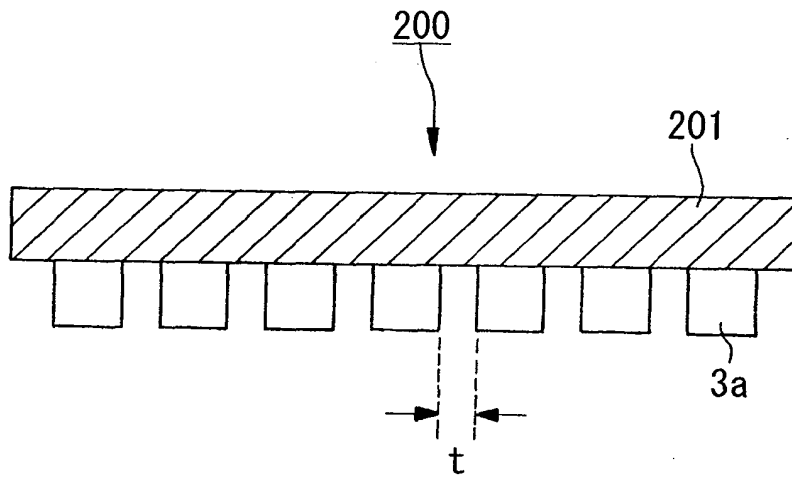


FIG. 89



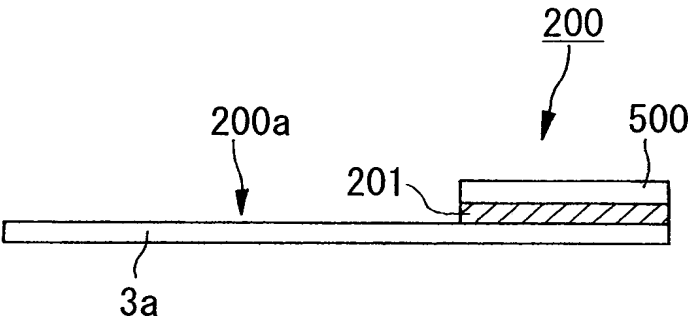
10076508-061902

FIG. 90



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FIG. 91



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FIG. 92

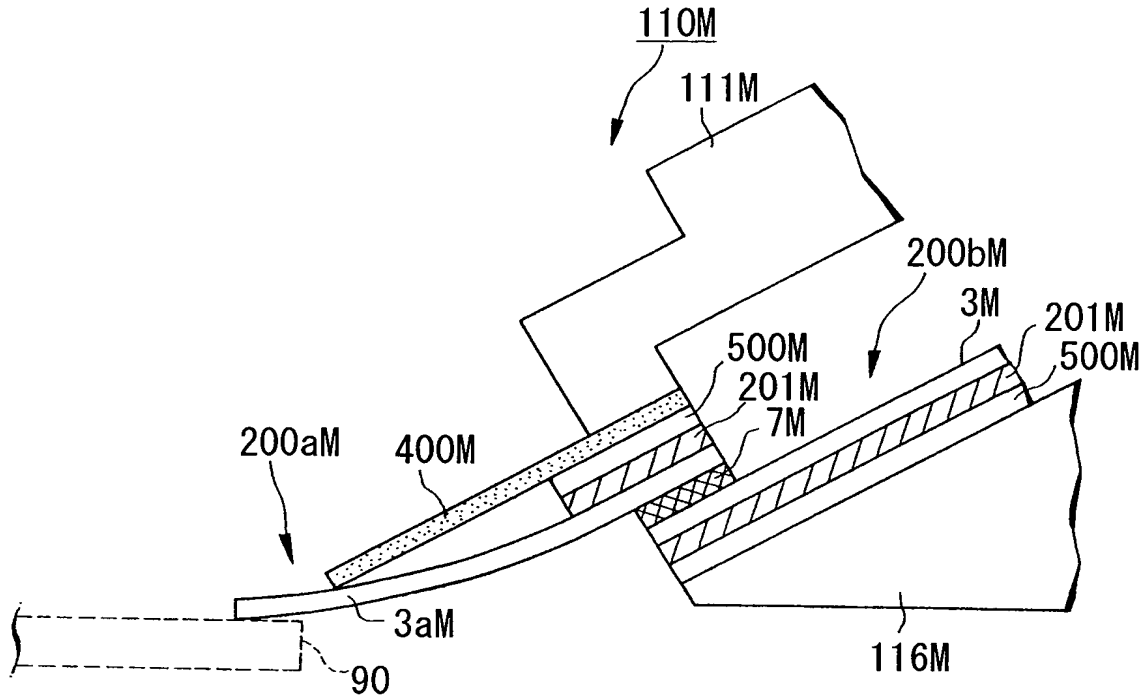


FIG. 93

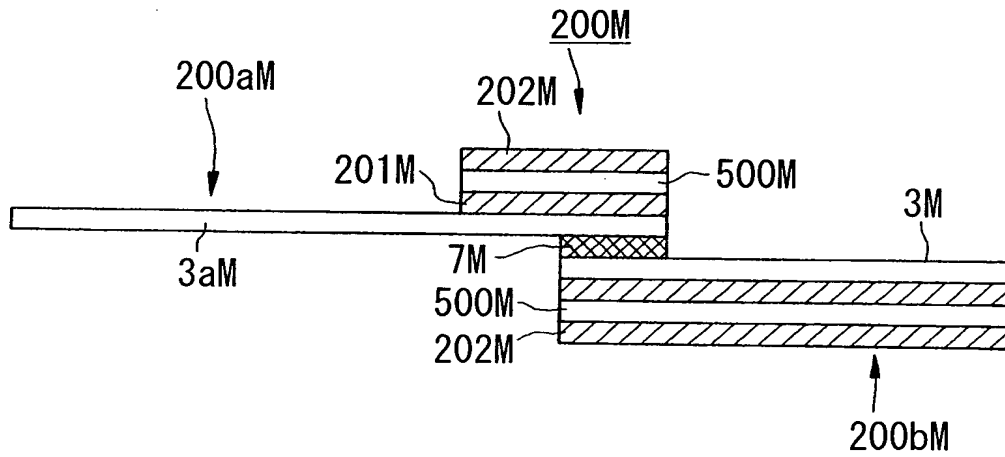


FIG. 94

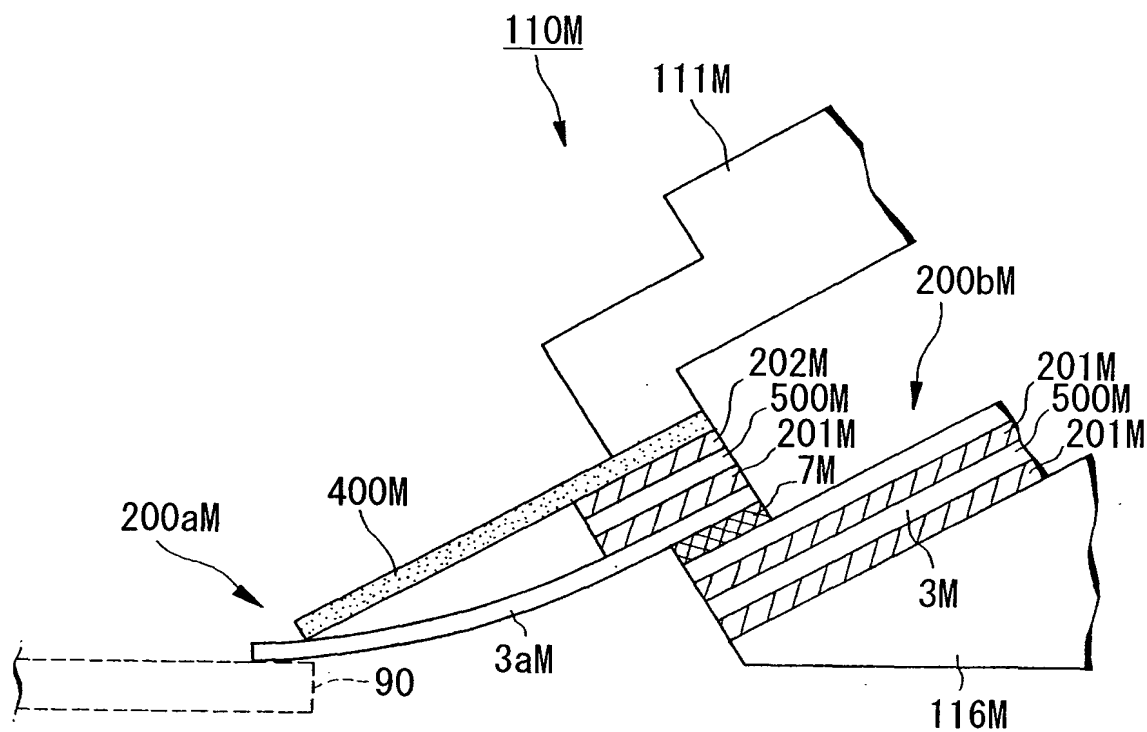
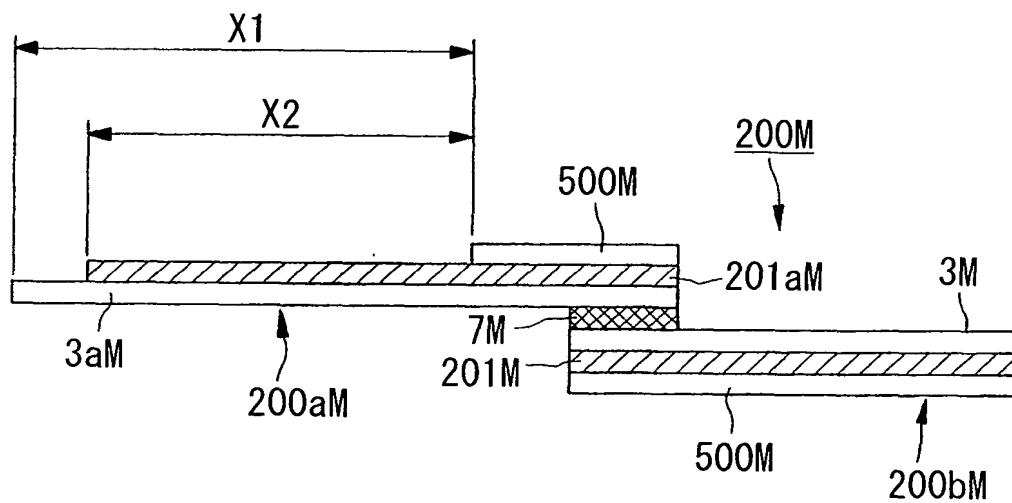


FIG. 95



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FIG. 96

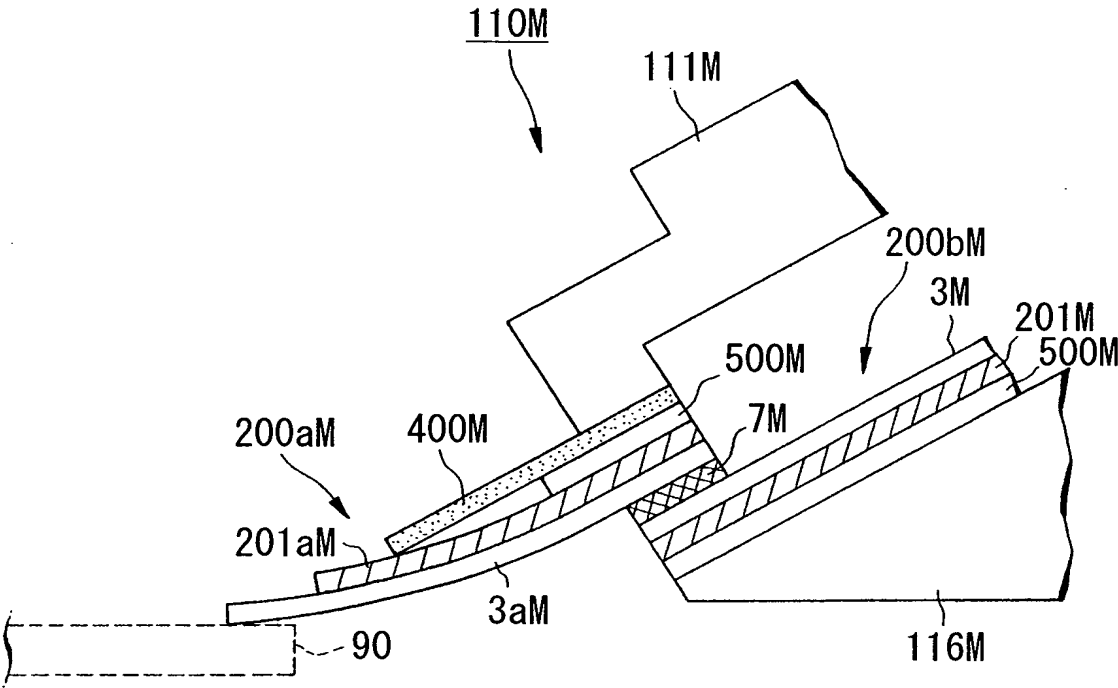


FIG. 97

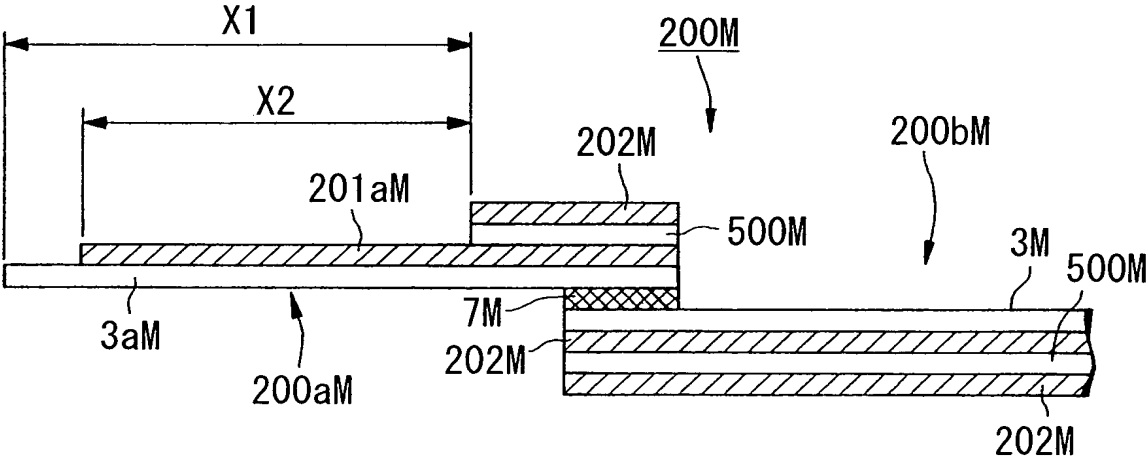
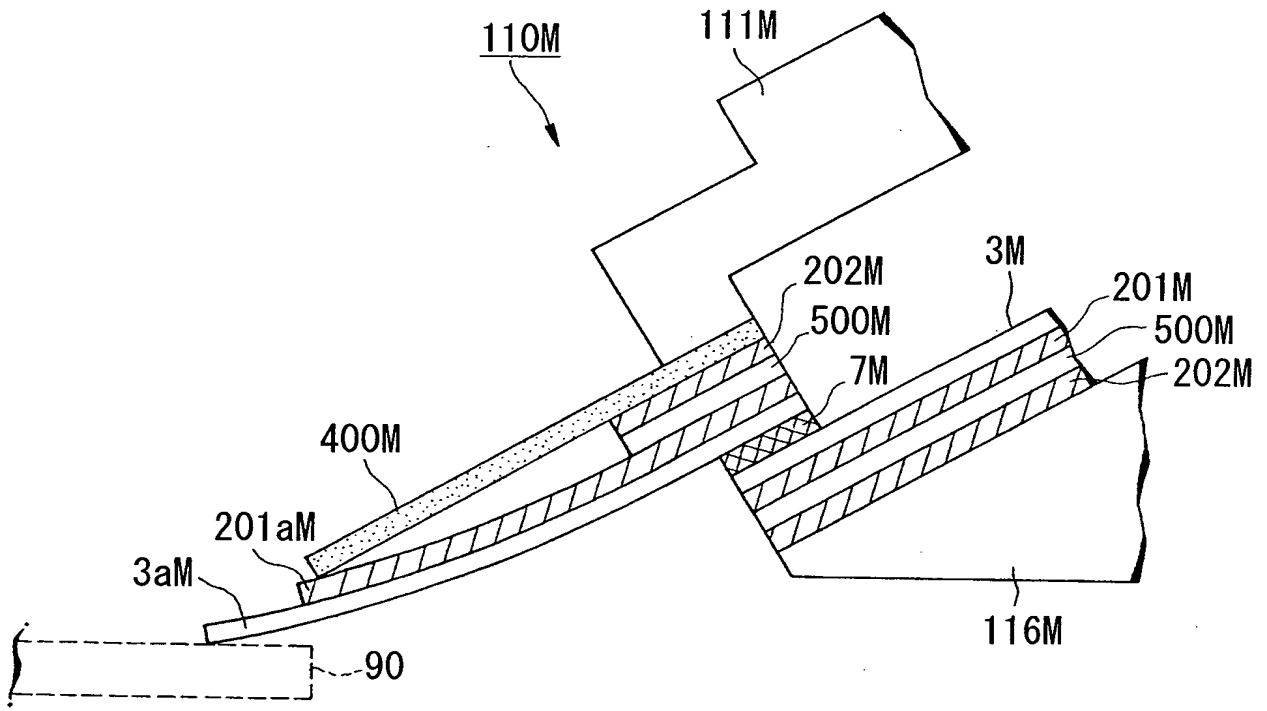
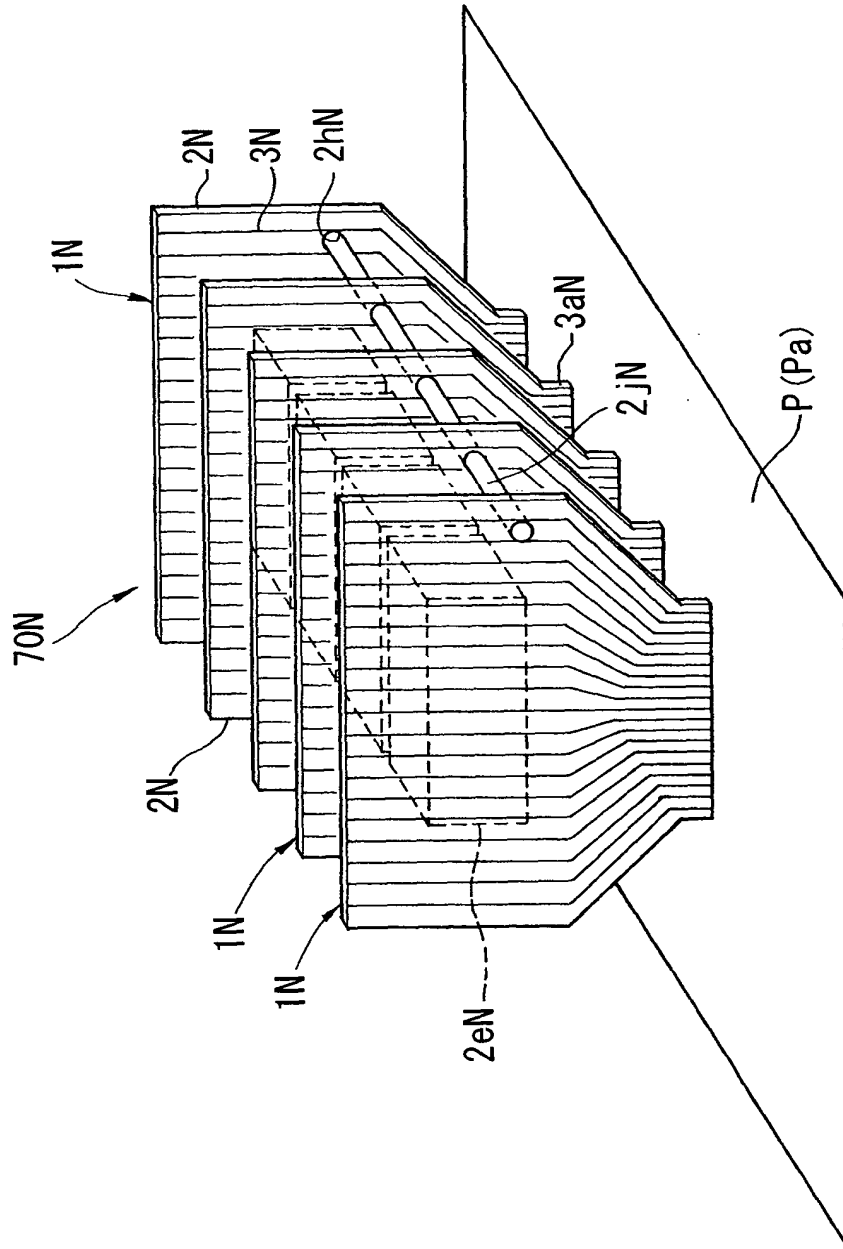


FIG. 98



10076508.061907

FIG. 99



206T50" 8059/00T

FIG. 100

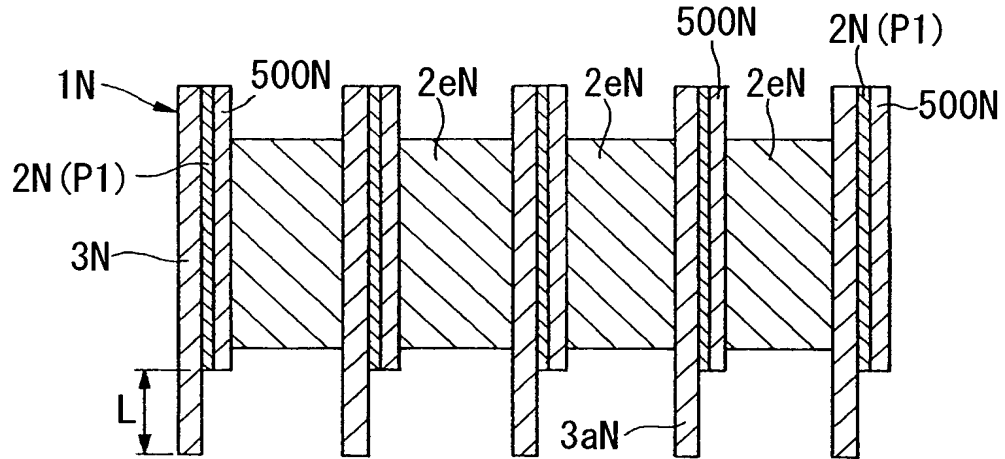


FIG. 101

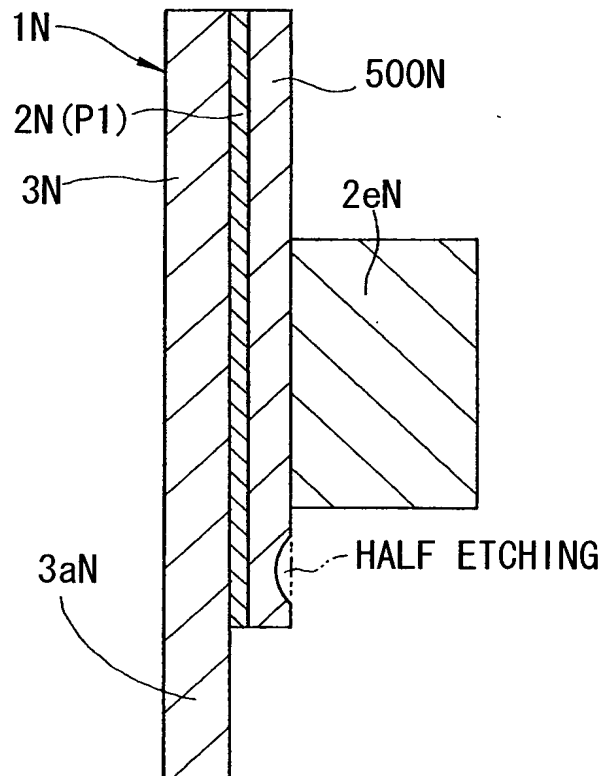
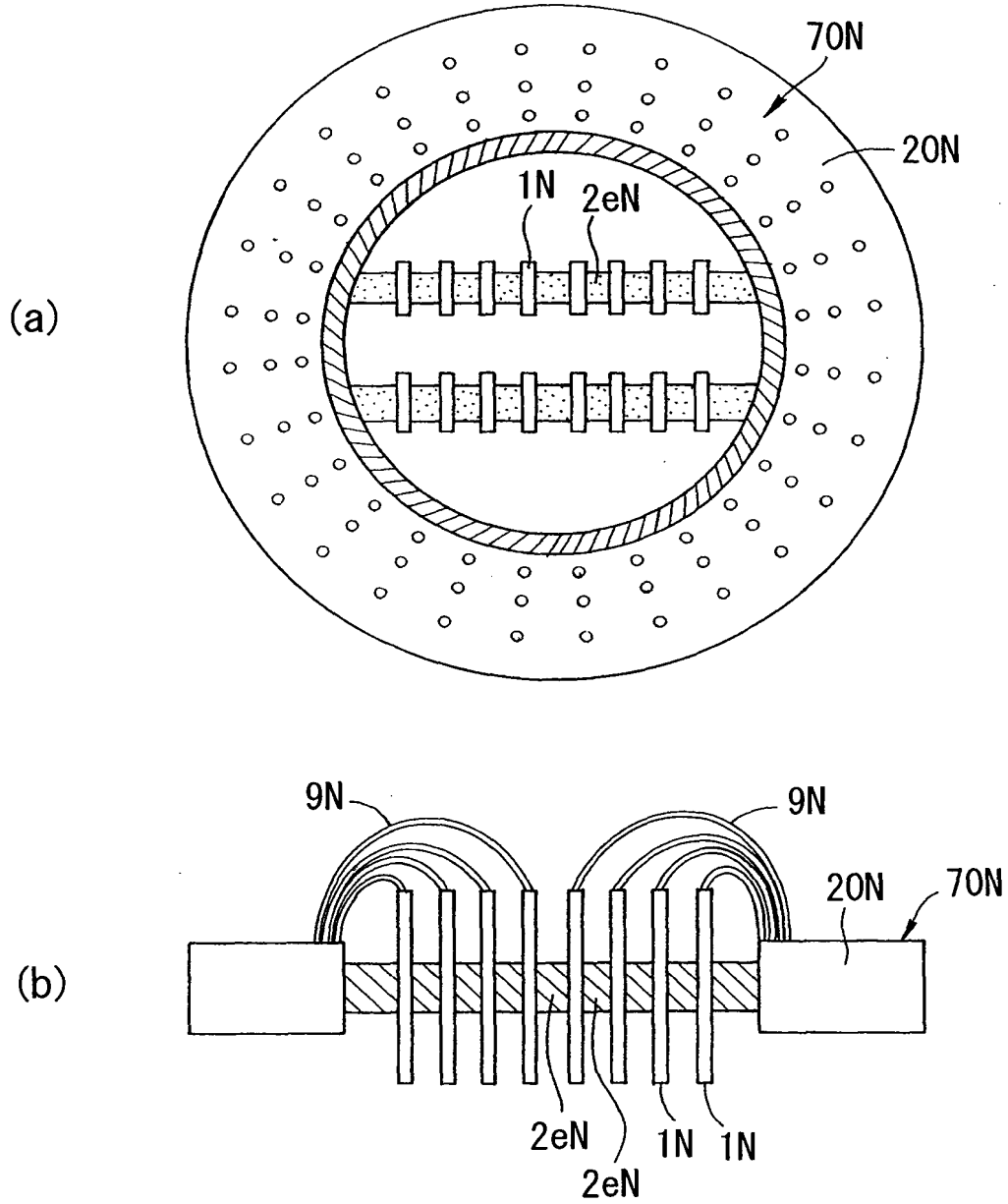
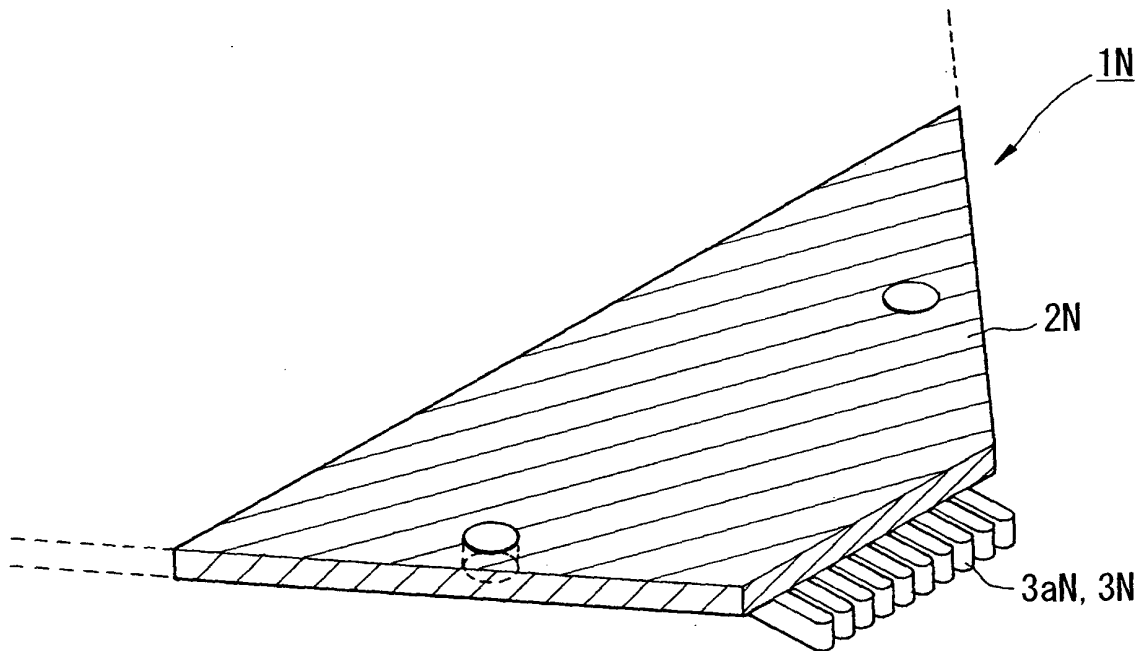


FIG. 102



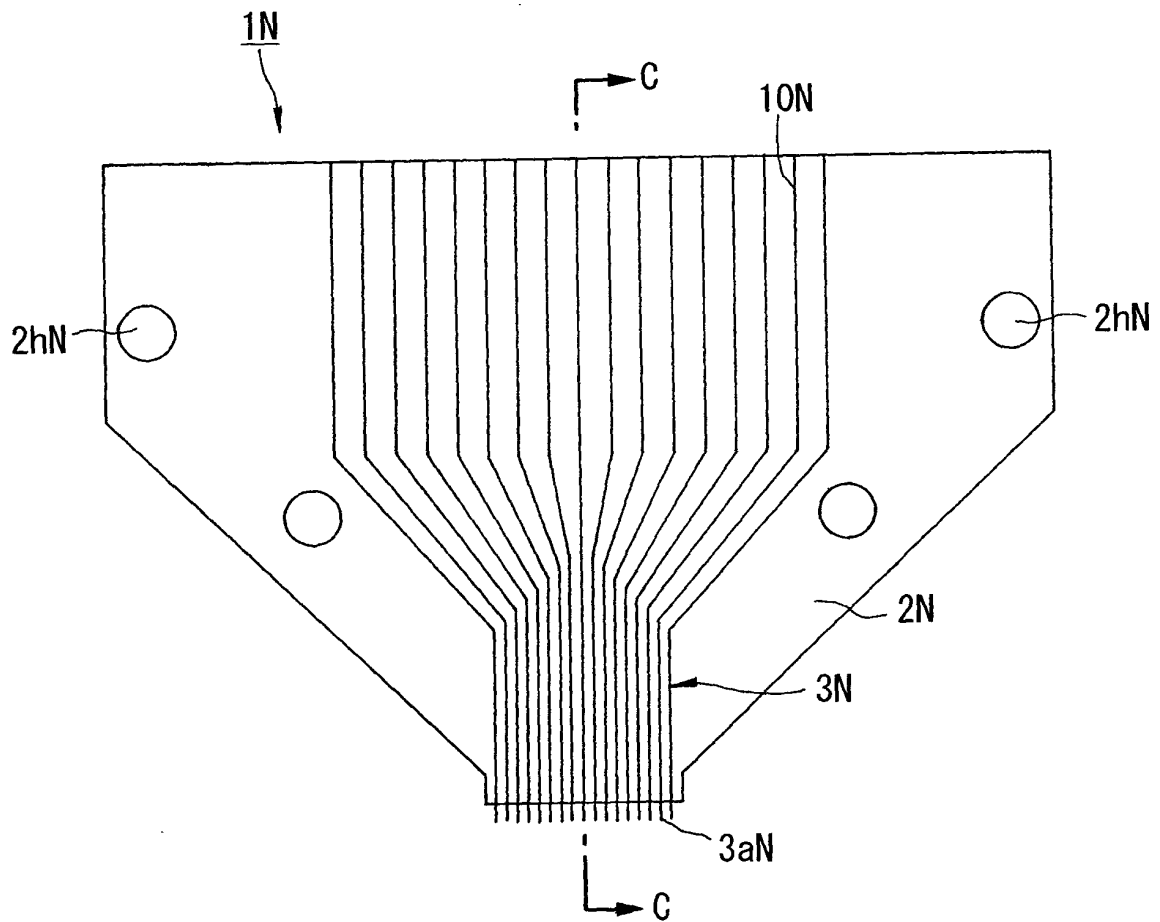
206T90" 805400T

FIG. 103



1006508.061901

FIG. 104



10076508-061902

FIG. 105

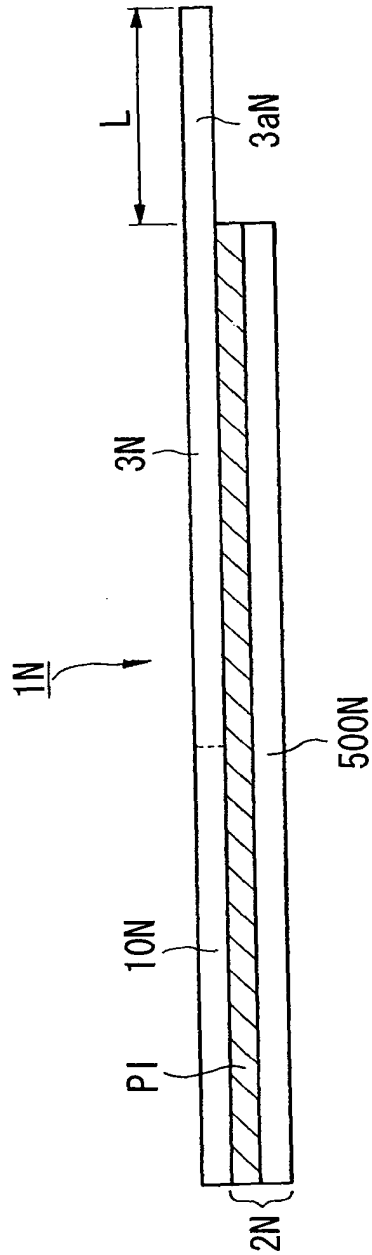


FIG. 106

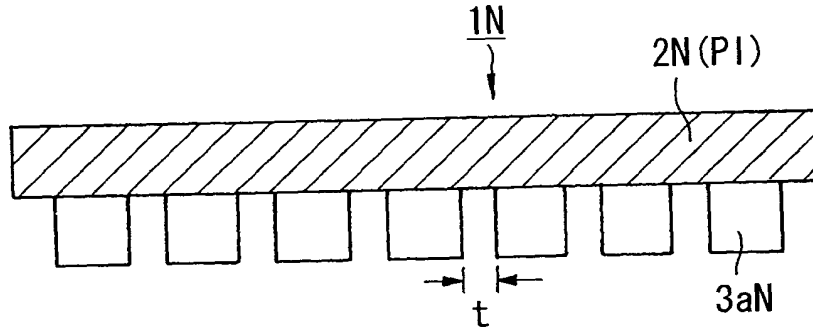
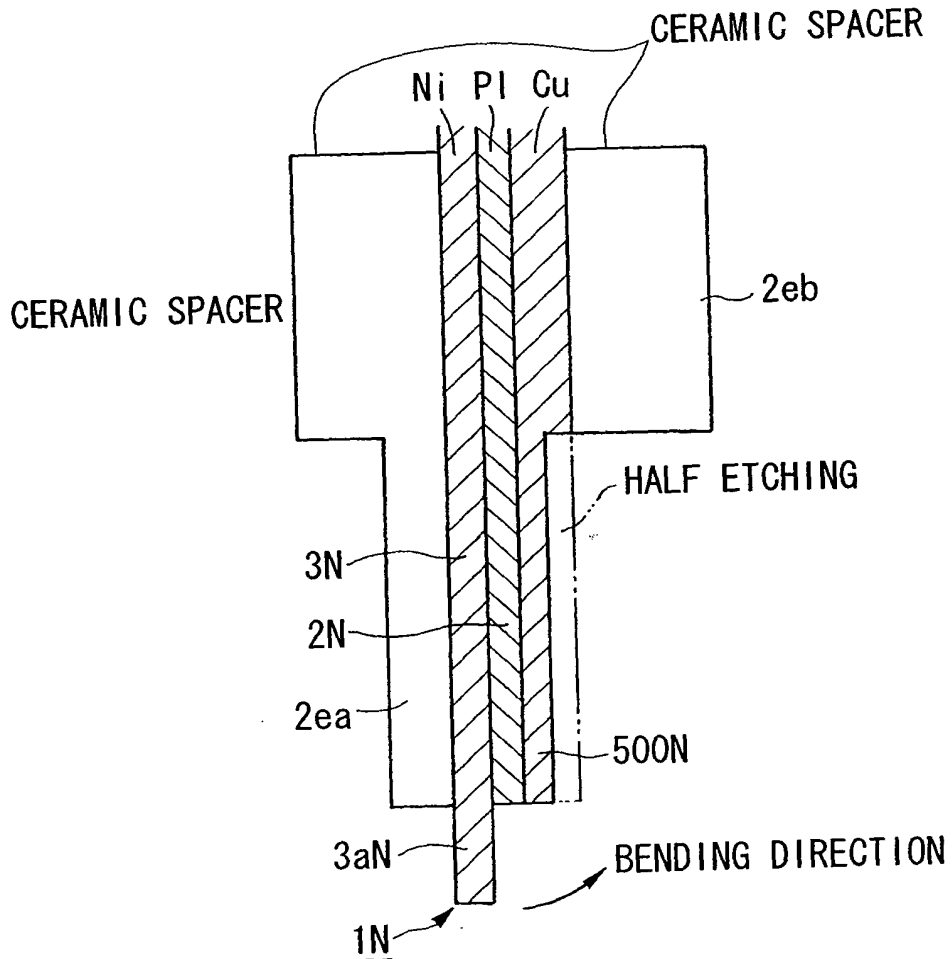


FIG. 107



200706508 061907

FIG. 108

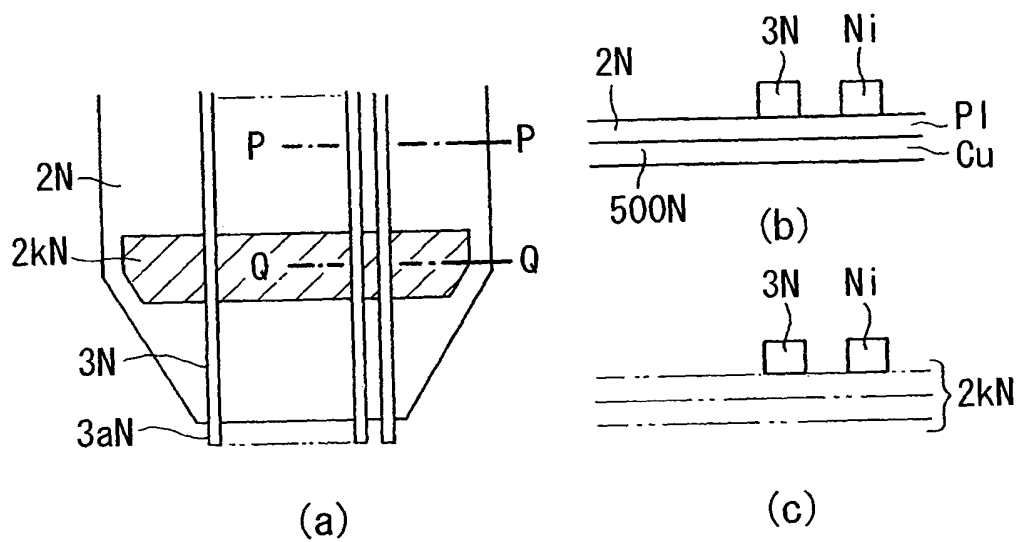
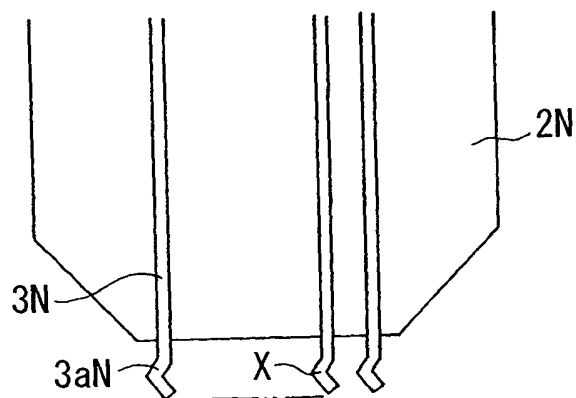
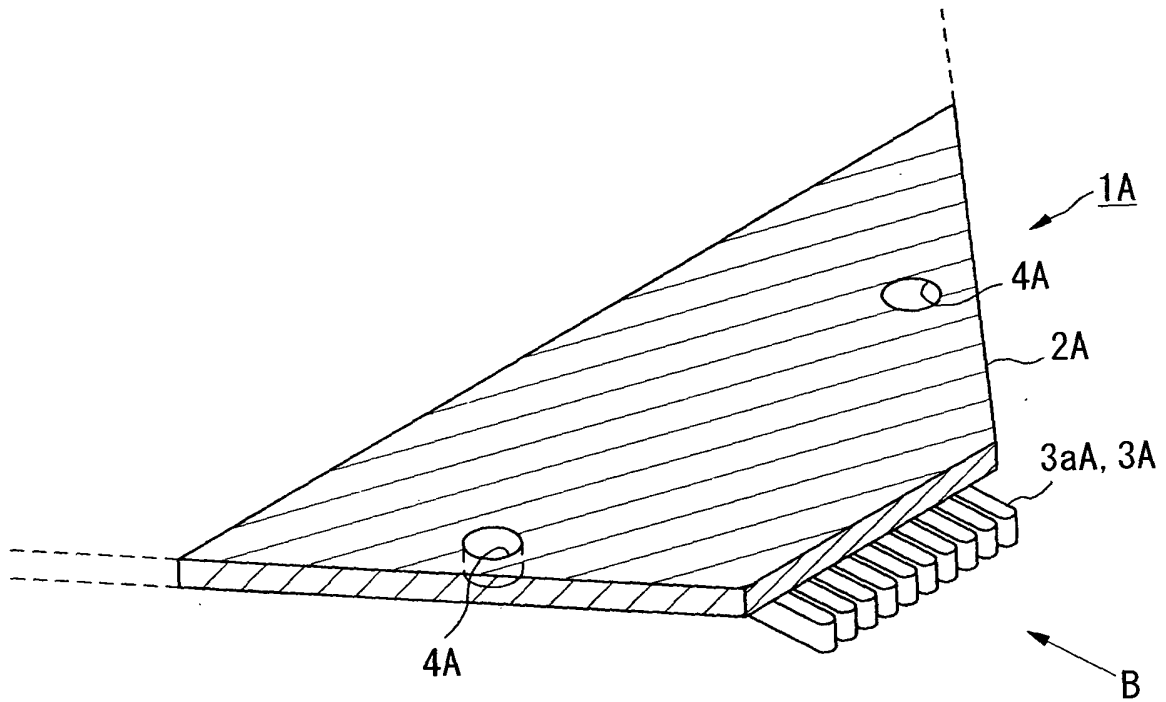


FIG. 109



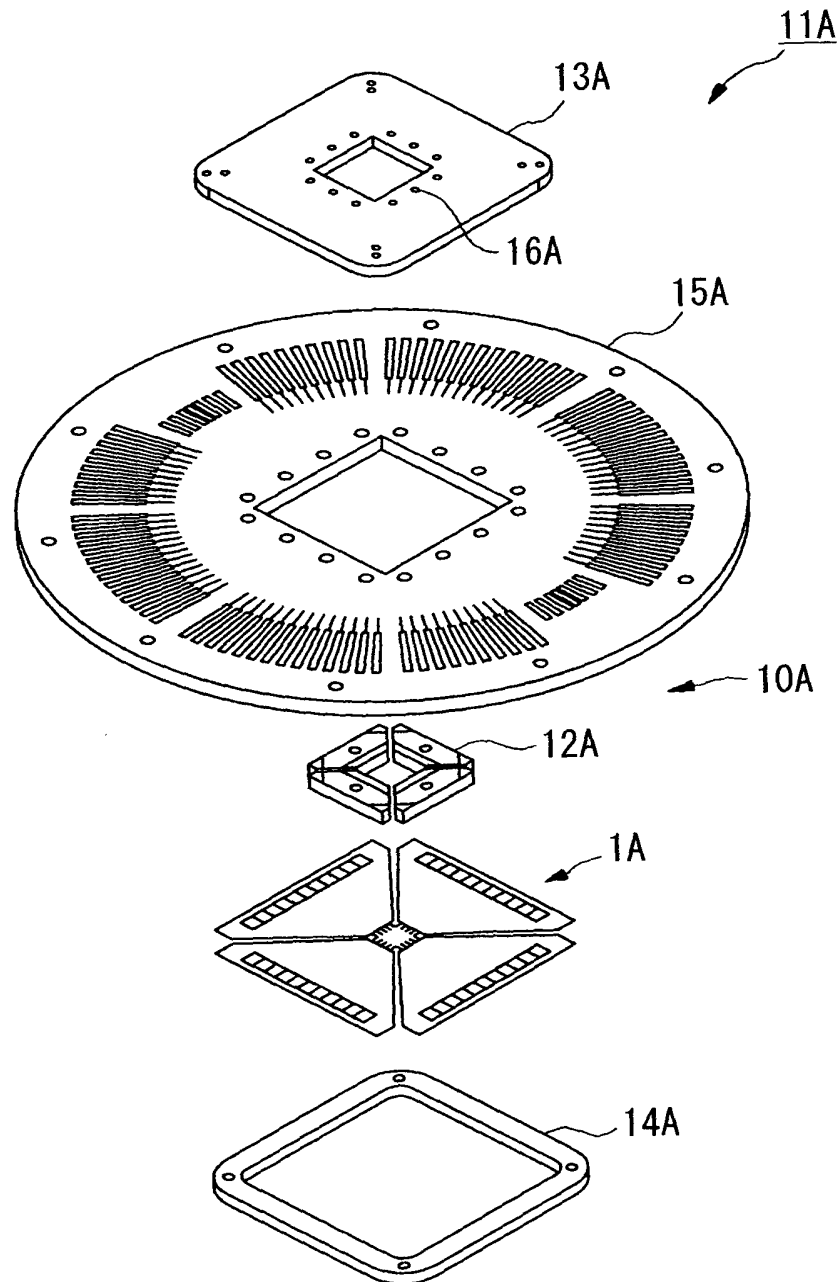
10076508-061902

FIG. 110



10076508-051902

FIG. 111



206T90" 8059/00T

FIG. 112

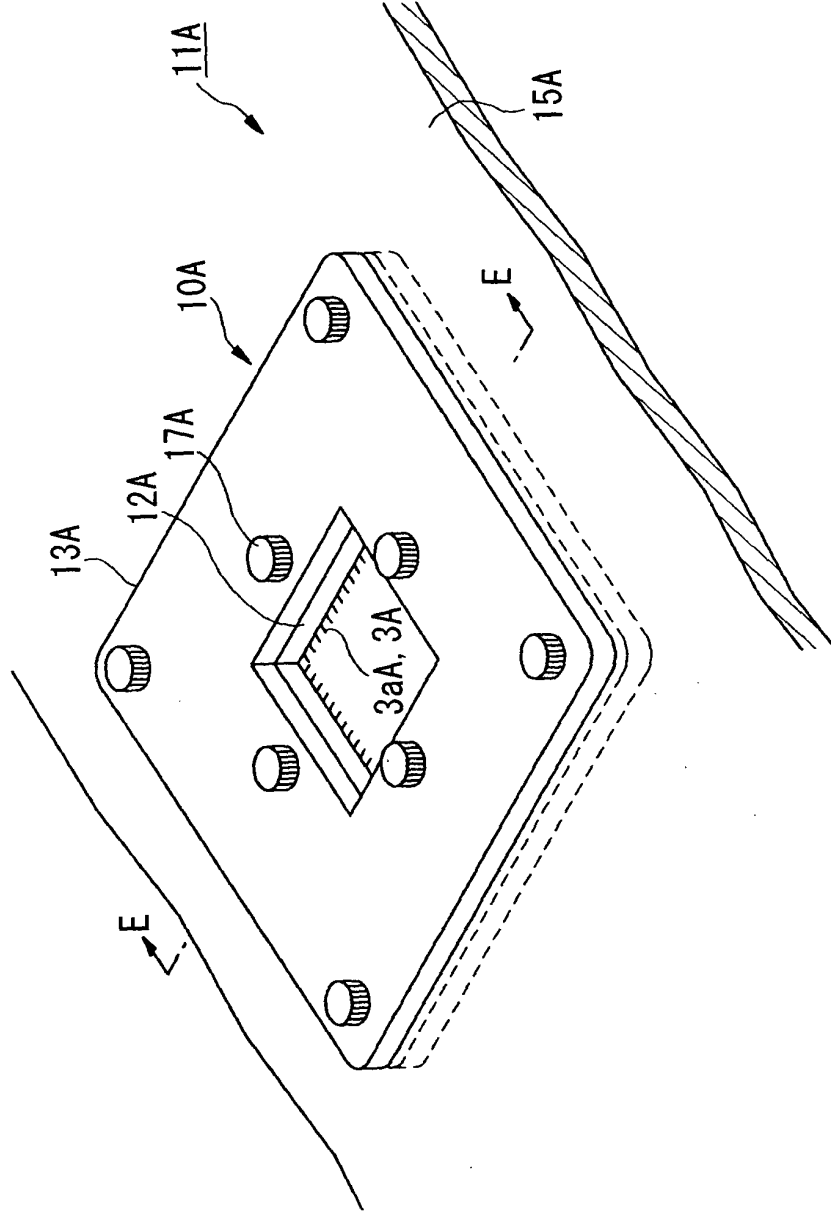


FIG. 113

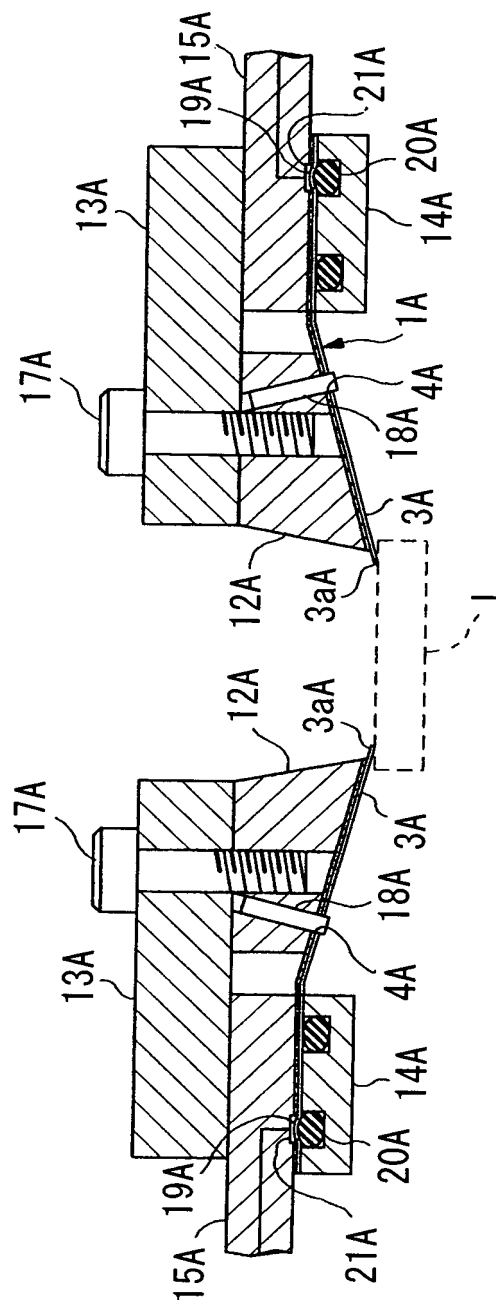
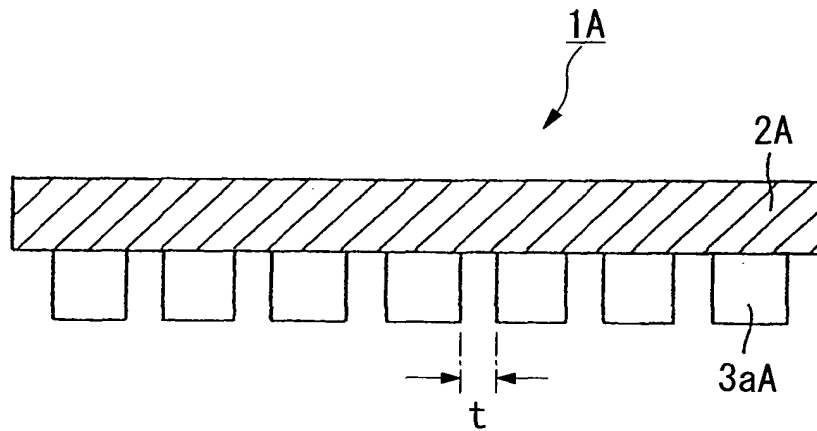
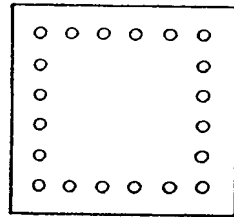


FIG. 114

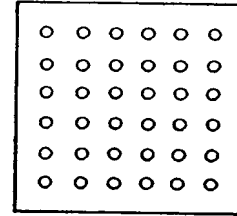


206F90" B059/00F

FIG. 115



PERIPHERALLY ARRANGED
TERMINALS



PLANARLY ARRANGED
TERMINALS

(a)

(b)

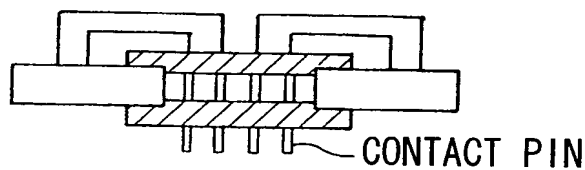
ARRANGEMENT OF ELECTRODE TERMINALS

FIG. 116



HORIZONTAL NEEDLE TYPE PROBE CARD

FIG. 117



VERTICAL NEEDLE TYPE PROBE CARD

10076508-061902